

### Application

- iNIC
- AP Router

The RT5350 SOC combines Ralink's 802.11n draft compliant 1T1R MAC/BBP/PA/RF, a high performance 360MHz MIPS24KEc CPU core, 5-ports integrated 10/100 Ethernet Switch/PHY and an USB Host/Device. With the RT5350, there are very few external components required for 2.4GHz 11n wireless products. The RT5350 employs Ralink 2nd generation 11n technologies for longer range and better throughput. The embedded high performance CPU can process advanced applications effortlessly, such as WIFI data processing without overloading the host processor. In addition, the RT5350 has rich hardware interfaces (SPI/ I2S/ I2C/ PCM/ UART/ USB) to enable many possible applications.

### Features

- ♦ Embedded 1T1R 2.4G CMOS RF
- ♦ Embedded 802.11n 1T1R MAC/BBP w/MLD enhancement
- ♦ Embedded PA/LNA
- ♦ 150Mbps PHY data rate
- ♦ 20Mhz/40Mhz channel width
- ♦ Legacy and high throughput modes
- ♦ Compressed Block ACK
- ♦ Bluetooth Co-existence
- ♦ Multiple BSSID (up to 16)
- ♦ WEP64/128, WPA, WPA2, WAPI engines
- ♦ QOS - WMM, WMM Power Save
- ♦ Hardware frame aggregation

- ♦ International Regulation - 802.11h TPC
- ♦ MIPS 24KEc 360Mhz with 32KB I cache/16KB D cache
- ♦ Support 16bit SDR SDRAM (up-to 64M bytes)
- ♦ Support boot from ROM, FLASH
- ♦ USB2.0 HOST/Device dual mode x1
- ♦ Embedded a 5-port 10/100Mbps Ethernet switch and a 5-port UTP PHY
- ♦ Support 5 10/100 UTP ports
- ♦ Slow speed I/O : GPIO, SPI, I2C, I2S, PCM, UART, and JTAG
- ♦ Package and I/O voltage
  - 12mm x 12mm TFBGA-196 Package
  - I/O : 3.3v I/O

### Order Information

| Part Number | Temp Range            | Package                                                |
|-------------|-----------------------|--------------------------------------------------------|
| RT5350F     | -10~55 <sup>0</sup> C | Green/ RoHS Compliant<br>TFBGA 196 ball<br>(12mmx12mm) |

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### Functional Block Diagram

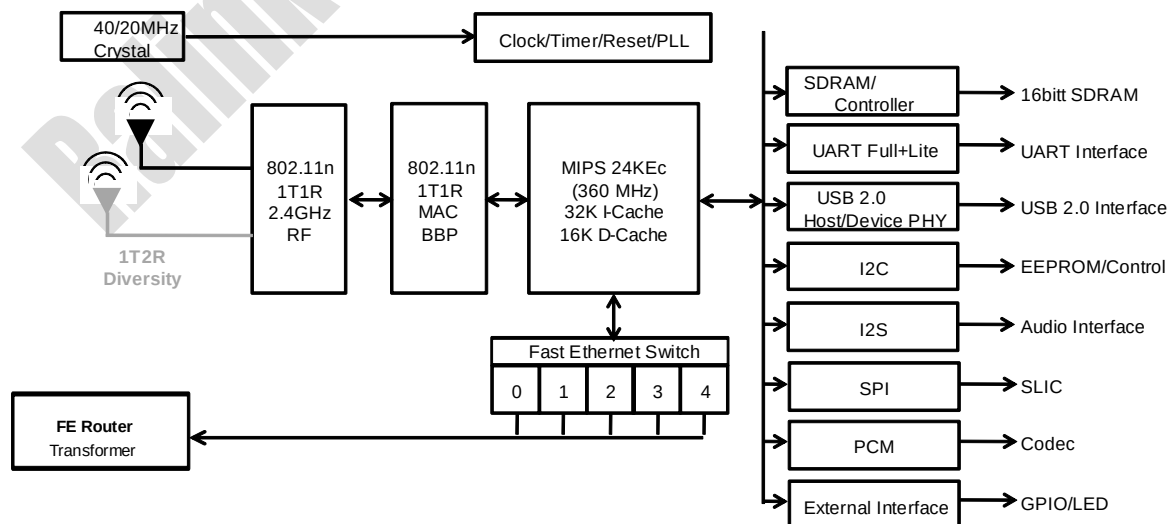


Fig. 1-1 RT5350 Functional Block Diagram

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## 1 Pin Description

### 1.1 196-Pins BGA Package Diagram

Top view (left portion)

|   | 1              | 2             | 3               | 4            | 5              | 6               | 7                 |
|---|----------------|---------------|-----------------|--------------|----------------|-----------------|-------------------|
| A | GND            | WL_RF0_2G_INP | WL_RF0_2G_INN   | GND          | WL_RF_BB1_V12A | WL_PLL_VC_CAP   | WL_PLL_X1         |
| B | WL_RF0_PA_V33P | GND           | WL_RF0_RF_V12A  | GND          | WL_RF0_IF_V12A | WL_PLL_V12A     | WL_PLL_X2         |
| C | WL_RF0_PA_OUTP | GND           | GND             | GND          | GND            | WL_VCO_VCO_V12A | WL_LDOPLL_OUT_V12 |
| D | WL_RF0_PA_OUTN | GND           | GND             | GND          | GND            | GND             | GND               |
| E | WL_RF0_PA_V33N | GND           | WL_RF0_PA1_V33A | GND          | GND            | GND             | GND               |
| F | GND            | GND           | GND             | GND          | SOC_IO_V33D    | GND             | GND               |
| G | VOUT_1P2       | LDO_V18A      | LDOSSEL         | COMP         | SOC_IO_V33D    | GND             | GND               |
| H | UGATE          | DCDC_V33A     | EXT_LDO_1P2     | FB           | SOC_CO_V12D    | GND             | GND               |
| J | LGATE          | DCDC_V33D     | SPI_MOSI        | DCD_N        | SOC_CO_V12D    | GND             | GND               |
| K | WLAN_LED_N     | TXD           | EPHY_LED0_N     | CTS_N        | EPHY_V33A      | EPHY_V33A       | EPHY_V33A         |
| L | EPHY_LED1_N    | SPI_CS1       | DSR_N           | EPHY_LED2_N  | EPHY_RXN_P0    | EPHY_RXN_P1     | EPHY_TXP_P2       |
| M | EPHY_LED3_N    | SPI_MISO      | RIN             | EPHY_LED4_N  | EPHY_RXP_P0    | EPHY_RXP_P1     | EPHY_TXN_P2       |
| N | SPI_CLK        | TXD2          | RXD             | DTR_N        | EPHY_TXN_P0    | EPHY_TXN_P1     | EPHY_RXN_P2       |
| P | SPI_CS0        | RTS_N         | RXD2            | EPHY_REF_RES | EPHY_TXP_P0    | EPHY_TXP_P1     | EPHY_RXP_P2       |

Top view (right portion)

| 8                | 9             | 10            | 11              | 12         | 13              | 14       |   |
|------------------|---------------|---------------|-----------------|------------|-----------------|----------|---|
| WL_LDORF_IN_VX   | WL_BG_V33A    | PLL_AVDD_V12A | JTAG_TRST_N     | JTAG_TCLK  | JTAG_TMS        | JTAG_TDI | A |
| WL_BG_RES_12K    | WL_ADC_V12    | PLL_DVDD_V12D | JTAG_TDO        | GPIO0      | I2C_SD          | I2C_SCLK | B |
| WL_LDORF_OUT_V12 | WL_RF_BB2_V12 | PORST_N       | MCKE            | MCAS_N     | MWE_N           | MCS1_N   | C |
| GND              | GND           | SOC_IO_V33D_1 | MD1             | MD2        | MD3             | MD4      | D |
| GND              | GND           | MD0           | MD5             | MD7        | MD9             | MD10     | E |
| GND              | SOC_CO_V12D   | SDRAM_IO_V33D | MD6             | MD8        | MD13            | MD15     | F |
| GND              | SOC_CO_V12D   | SDRAM_IO_V33D | MD11            | MD12       | MD14            | MA0      | G |
| GND              | SOC_CO_V12D   | SDRAM_IO_V33D | MA3             | MA2        | MA1             | MCLK     | H |
| GND              | GND           | MDQM0         | MA9             | MA6        | MA5             | MA4      | J |
| EPHY_V33A        | GND           | GND           | MCS0_N          | MA11       | MA8             | MA7      | K |
| EPHY_RXP_P3      | EPHY_TXP_P4   | GND           | MRAS_N          | MBA0       | MA12            | MA10     | L |
| EPHY_RXN_P3      | EPHY_TXN_P4   | GND           | GND             | GND        | MDQM1           | MBA1     | M |
| EPHY_TXN_P3      | EPHY_RXN_P4   | GND           | UPHY0_VDDA_V33A | UPHY0_PADM | GND             | GND      | N |
| EPHY_TXP_P3      | EPHY_RXP_P4   | GND           | UPHY0_VRES      | UPHY0_PADP | UPHY0_VDDL_V12D | GND      | P |

## 1.2 Pin Description

| Pin                           | Name         | I/O/IPU/IPD | Driving | Description                                                      |
|-------------------------------|--------------|-------------|---------|------------------------------------------------------------------|
| JTAG interfaces : 5 pins      |              |             |         |                                                                  |
| A11                           | JTAG_TRST_N  | I, IPU      | 4mA     | JTAG TRST (active low)                                           |
| A12                           | JTAG_TCLK    | I, IPD      | 4mA     | JTAG TCLK                                                        |
| A13                           | JTAG_TMS     | I, IPD      | 4mA     | JTAG TMS                                                         |
| A14                           | JTAG_TDI     | I, IPD      | 4mA     | JTAG TDI                                                         |
| B11                           | JTAG_TDO     | O, IPD      | 4mA     | JTAG TDO                                                         |
| UART Lite interface : 2 pins  |              |             |         |                                                                  |
| P3                            | RXD2         | I, IPD      | 4mA     | UART Lite RXD                                                    |
| N2                            | TXD2         | O, IPD      | 4mA     | UART Lite TXD                                                    |
| UART Full interface : 8 pins  |              |             |         |                                                                  |
| N3                            | RXD          | I, IPD      | 4mA     | UART RXD.                                                        |
| M3                            | RIN          | I, IPD      | 4mA     | UART RIN.                                                        |
| K4                            | CTS_N        | I, IPD      | 4mA     | UART CTS_N.                                                      |
| L3                            | DSR_N        | I, IPD      | 4mA     | UART DSR_N.                                                      |
| J4                            | DCD_N        | I, IPD      | 4mA     | UART DCD_N.                                                      |
| K2                            | TXD          | O, IPD      | 4mA     | UART TXD.                                                        |
| N4                            | DTR_N        | O, IPD      | 4mA     | UART DTR.                                                        |
| P2                            | RTS_N        | O, IPD      | 4mA     | UART RTS.                                                        |
| SPI/EEPROM interface : 5 pins |              |             |         |                                                                  |
| M2                            | SPI_MISO     | I, IPD      | 4mA     | SPI master in slave out                                          |
| J3                            | SPI_MOSI     | O, IPD      | 4mA     | SPI master out slave in                                          |
| N1                            | SPI_CLK      | O, IPD      | 4mA     | SPI clock                                                        |
| P1                            | SPI_CS0      | O, IPD      | 4mA     | SPI chip select0                                                 |
| L2                            | SPI_CS1      | O, IPD      | 4mA     | SPI chip select1                                                 |
| I2C interface: 2 pins         |              |             |         |                                                                  |
| B14                           | I2C_SCLK     | I/O, IPU    | 8mA     | I2C Clock                                                        |
| B13                           | I2C_SD       | O, IPU      | 8mA     | I2C Data                                                         |
| GPIO interface: 1 pins        |              |             |         |                                                                  |
| B12                           | GPIO0        | I/O, IPD    | 8mA     | GPIO0                                                            |
| 5-Port PHY : 26 pins          |              |             |         |                                                                  |
| K3                            | EPHY_LED0_N  | O, IPD      | 4mA     | 10/100 PHY Port #0 activity LED                                  |
| L1                            | EPHY_LED1_N  | O, IPD      | 4mA     | 10/100 PHY Port #1 activity LED                                  |
| L4                            | EPHY_LED2_N  | O, IPD      | 4mA     | 10/100 PHY Port #2 activity LED                                  |
| M1                            | EPHY_LED3_N  | O, IPD      | 4mA     | 10/100 PHY Port #3 activity LED                                  |
| M4                            | EPHY_LED4_N  | O, IPD      | 4mA     | 10/100 PHY Port #4 activity LED                                  |
| P4                            | EPHY_REF_RES | A           |         | Connect to an external resistor to provide accurate bias current |
| L5                            | EPHY_RXN_P0  | I           |         | 10/100 PHY Port #0 RXN                                           |
| M5                            | EPHY_RXP_P0  | I           |         | 10/100 PHY Port #0 RXP                                           |
| N5                            | EPHY_TXN_P0  | O           |         | 10/100 PHY Port #0 TXN                                           |
| P5                            | EPHY_TXP_P0  | O           |         | 10/100 PHY Port #0 TXP                                           |
| L6                            | EPHY_RXN_P1  | I           |         | 10/100 PHY Port #1 RXN                                           |
| M6                            | EPHY_RXP_P1  | I           |         | 10/100 PHY Port #1 RXP                                           |
| N6                            | EPHY_TXN_P1  | O           |         | 10/100 PHY Port #1 TXN                                           |
| P6                            | EPHY_TXP_P1  | O           |         | 10/100 PHY Port #1 TXP                                           |
| N7                            | EPHY_RXN_P2  | I           |         | 10/100 PHY Port #2 RXN                                           |
| P7                            | EPHY_RXP_P2  | I           |         | 10/100 PHY Port #2 RXP                                           |
| M7                            | EPHY_TXN_P2  | O           |         | 10/100 PHY Port #2 TXN                                           |
| L7                            | EPHY_TXP_P2  | O           |         | 10/100 PHY Port #2 TXP                                           |

| Pin                        | Name            | I/O/IPU/IPD | Driving | Description                                                             |
|----------------------------|-----------------|-------------|---------|-------------------------------------------------------------------------|
| M8                         | EPHY_RXN_P3     | I           |         | 10/100 PHY Port #3 RXN                                                  |
| L8                         | EPHY_RXP_P3     | I           |         | 10/100 PHY Port #3 RXP                                                  |
| N8                         | EPHY_TXN_P3     | O           |         | 10/100 PHY Port #3 TXN                                                  |
| P8                         | EPHY_TXP_P3     | O           |         | 10/100 PHY Port #3 TXP                                                  |
| N9                         | EPHY_RXN_P4     | I           |         | 10/100 PHY Port #4 RXN                                                  |
| P9                         | EPHY_RXP_P4     | I           |         | 10/100 PHY Port #4 RXP                                                  |
| M9                         | EPHY_TXN_P4     | O           |         | 10/100 PHY Port #4 TXN                                                  |
| L9                         | EPHY_TXP_P4     | O           |         | 10/100 PHY Port #4 TXP                                                  |
| Misc signals : 2 pins      |                 |             |         |                                                                         |
| C10                        | PORST_N         | I, IPU      | 2mA     | Power on reset                                                          |
| K1                         | WLAN_LED_N      | O, IPD      | 4mA     | WLAN Activity LED                                                       |
| USB PHY interface : 5 pins |                 |             |         |                                                                         |
| N11                        | UPHY0_VDDA_V33A | P           |         | 3.3v USB PHY analog power supply                                        |
| P13                        | UPHY0_VDDL_V12D | P           |         | 1.2v USB PHY digital power supply                                       |
| P11                        | UPHY0_VRES      | I/O         |         | Connect to an external 8.2K Ohm resistor for band-gap reference circuit |
| N12                        | UPHY0_PADM      | I/O         |         | USB data pin Data-                                                      |
| P12                        | UPHY0_PADP      | I/O         |         | USB data pin Data+                                                      |
| SDRAM Interface : 40 pins  |                 |             |         |                                                                         |
| F14                        | MD15            | I/O         | 4/8mA   | SDRAM Data bit #15                                                      |
| G13                        | MD14            | I/O         | 4/8mA   | SDRAM Data bit #14                                                      |
| F13                        | MD13            | I/O         | 4/8mA   | SDRAM Data bit #13                                                      |
| G12                        | MD12            | I/O         | 4/8mA   | SDRAM Data bit #12                                                      |
| G11                        | MD11            | I/O         | 4/8mA   | SDRAM Data bit #11                                                      |
| E14                        | MD10            | I/O         | 4/8mA   | SDRAM Data bit #10                                                      |
| E13                        | MD9             | I/O         | 4/8mA   | SDRAM Data bit #9                                                       |
| F12                        | MD8             | I/O         | 4/8mA   | SDRAM Data bit #8                                                       |
| E12                        | MD7             | I/O         | 4/8mA   | SDRAM Data bit #7                                                       |
| F11                        | MD6             | I/O         | 4/8mA   | SDRAM Data bit #6                                                       |
| E11                        | MD5             | I/O         | 4/8mA   | SDRAM Data bit #5                                                       |
| D14                        | MD4             | I/O         | 4/8mA   | SDRAM Data bit #4                                                       |
| D13                        | MD3             | I/O         | 4/8mA   | SDRAM Data bit #3                                                       |
| D12                        | MD2             | I/O         | 4/8mA   | SDRAM Data bit #2                                                       |
| D11                        | MD1             | I/O         | 4/8mA   | SDRAM Data bit #1                                                       |
| E10                        | MD0             | I/O         | 4/8mA   | SDRAM Data bit #0                                                       |
| L13                        | MA12            | I/O         | 4/8mA   | SDRAM Address bit #12                                                   |
| K12                        | MA11            | I/O         | 4/8mA   | SDRAM Address bit #11                                                   |
| L14                        | MA10            | I/O         | 4/8mA   | SDRAM Address bit #10                                                   |
| J11                        | MA9             | I/O         | 4/8mA   | SDRAM Address bit #9                                                    |
| K13                        | MA8             | I/O         | 4/8mA   | SDRAM Address bit #8                                                    |
| K14                        | MA7             | I/O         | 4/8mA   | SDRAM Address bit #7                                                    |
| J12                        | MA6             | I/O         | 4/8mA   | SDRAM Address bit #6                                                    |
| J13                        | MA5             | I/O         | 4/8mA   | SDRAM Address bit #5                                                    |
| J14                        | MA4             | I/O         | 4/8mA   | SDRAM Address bit #4                                                    |
| H11                        | MA3             | I/O         | 4/8mA   | SDRAM Address bit #3                                                    |
| H12                        | MA2             | I/O         | 4/8mA   | SDRAM Address bit #2                                                    |
| H13                        | MA1             | I/O         | 4/8mA   | SDRAM Address bit #1                                                    |
| G14                        | MA0             | I/O         | 4/8mA   | SDRAM Address bit #0                                                    |
| M14                        | MBA1            | I/O         | 4/8mA   | SDRAM MBA #1                                                            |
| L12                        | MBA0            | I/O         | 4/8mA   | SDRAM MBA #0                                                            |



| Pin                                                | Name            | I/O/IPU/IPD | Driving | Description                                                                                                         |
|----------------------------------------------------|-----------------|-------------|---------|---------------------------------------------------------------------------------------------------------------------|
| L11                                                | MRAS_N          | I/O         | 4/8mA   | SDRAM MRAS_N                                                                                                        |
| C12                                                | MCAS_N          | I/O         | 4/8mA   | SDRAM MCAS_N                                                                                                        |
| C13                                                | MWE_N           | I/O         | 4/8mA   | SDRAM MWE_N                                                                                                         |
| H14                                                | MCLK            | I/O         | 8/12mA  | SDRAM MCK                                                                                                           |
| C11                                                | MCKE            | I/O         | 4/8mA   | SDRAM MCKE                                                                                                          |
| M13                                                | MDQM1           | I/O         | 4/8mA   | SDRAM MDQM#1                                                                                                        |
| J10                                                | MDQM0           | I/O         | 4/8mA   | SDRAM MDQM#0                                                                                                        |
| K11                                                | MCS0_N          | I/O         | 4/8mA   | SDRAM MCS0_N                                                                                                        |
| C14                                                | MCS1_N          | I/O         | 4/8mA   | SDRAM MCS1_N                                                                                                        |
| LDO pins : 10 pins                                 |                 |             |         |                                                                                                                     |
| G2                                                 | LDO_V18A        | P           |         | 1.8v power input for internal MOS                                                                                   |
| G1                                                 | VOOUT_1P2       | P           |         | 1.2v regulation output                                                                                              |
| G3                                                 | LDOSEL          | I           |         | Internal/External LDO Select<br>default: floating, use internal<br>tie to 3.3: use external                         |
| H3                                                 | EXT_LDO_1P2     | P           |         | Gate drive for external BJT                                                                                         |
| H2                                                 | DCDC_V33A       | P           |         | 3.3v analog power                                                                                                   |
| G4                                                 | COMP            | A           |         | This pin is the error amplifier<br>output and combination with the<br>FB pin, to compensate the voltage-<br>control |
| H4                                                 | FB              | A           |         | Programmable feedback reference<br>voltage for SW regulator and<br>compensation network of the error<br>amplifier   |
| H1                                                 | UGATE           | A           |         | Gate drive for external upper<br>MOSFET                                                                             |
| J1                                                 | LGATE           | A           |         | Gate drive for external lower<br>MOSFET                                                                             |
| J2                                                 | DCDC_V33D       | P           |         | 3.3v power supply only for gate<br>driver of SW (I <sub>peak</sub> <200mA;<br>I <sub>avg</sub> <20mA)               |
| PLL interface: 2 pins                              |                 |             |         |                                                                                                                     |
| B10                                                | PLL_DVDD_V12D   | P           |         | 1.2V digital power supply to PLL                                                                                    |
| A10                                                | PLL_AVDD_V12A   | P           |         | 1.2V analog power supply to PLL                                                                                     |
| RF interface, related LDO and power pins : 22 pins |                 |             |         |                                                                                                                     |
| A2                                                 | WL_RF0_2G_INP   | I           |         | 2.4GHz RX0 input (positive)                                                                                         |
| A3                                                 | WL_RF0_2G_INN   | I           |         | 2.4GHz RX0 input (negative)                                                                                         |
| B1                                                 | WL_RF0_PA_V33P  | P           |         | 3.3V Supply for RF channel 0                                                                                        |
| C1                                                 | WL_RF0_PA_OUTP  | O           |         | 2.4GHz TX PA output (negative)                                                                                      |
| D1                                                 | WL_RF0_PA_OUTN  | O           |         | 2.4GHz TX0 output (negative)                                                                                        |
| E1                                                 | WL_RF0_PA_V33N  | P           |         | 3.3V Supply for RF channel 0                                                                                        |
| E3                                                 | WL_RF0_PA1_V33A | P           |         | 3.3V Supply for RF0 PA1                                                                                             |
| B5                                                 | WL_RF0_IF_V12A  | P           |         | 1.2V Supply for IF0                                                                                                 |
| B3                                                 | WL_RF0_RF_V12A  | P           |         | 1.2V Supply for RF0                                                                                                 |
| B9                                                 | WL_ADC_V12      | P           |         | 1.2V supply for ADC analog blocks                                                                                   |
| A5                                                 | WL_RF_BB1_V12A  | P           |         | 1.2V Supply for analog baseband                                                                                     |
| C9                                                 | WL_RF_BB2_V12A  | P           |         | 1.2V Supply for analog baseband                                                                                     |
| B8                                                 | WL_BG_RES_12K   | I/O         |         | External reference resistor (12K<br>ohm)                                                                            |
| A9                                                 | WL_BG_V33A      | P           |         | 3.3V supply for band gap reference                                                                                  |

| Pin                                                                                                                                                                                                                   | Name              | I/O/IPU/IPD | Driving        | Description                                |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------|-------------|----------------|--------------------------------------------|
| C8                                                                                                                                                                                                                    | WL_LDORF_OUT_V12  | O           |                | LDO 1.2V 200mA output for RF core          |
| C7                                                                                                                                                                                                                    | WL_LDOPLL_OUT_V12 | O           |                | LDO 1.2V 200mA output for PLL core         |
| A8                                                                                                                                                                                                                    | WL_LDORF_IN_VX    | I           |                | LDO 1.5~2V 300mA input for RF core and PLL |
| A7                                                                                                                                                                                                                    | WL_PLL_X1         | I           |                | Crystal oscillator input                   |
| B7                                                                                                                                                                                                                    | WL_PLL_X2         | O           |                | Crystal oscillator output                  |
| B6                                                                                                                                                                                                                    | WL_PLL_V12A       | P           |                | 1.2V Supply for PL                         |
| A6                                                                                                                                                                                                                    | WL_PLL_VC_CAP     | I/O         |                | PLL external loop filter                   |
| C6                                                                                                                                                                                                                    | WL_VCO_VCO_V12A   | P           |                | 1.2V Supply for VCO output buffer          |
| Other power pins : 14 pins                                                                                                                                                                                            |                   |             |                |                                            |
| F5,G5,D10                                                                                                                                                                                                             | SOC_IO_V33D       | P           |                | 3.3v digital I/O power supply              |
| F10,G10,H10                                                                                                                                                                                                           | SDRAM_IO_V33D     | P           |                | 3.3v/1.8v SDRAM I/O power supply           |
| H5,J5,F9,G9,H9                                                                                                                                                                                                        | SOC_CO_V12D       | P           |                | 1.2v digital core power supply             |
| K5,K6,K7                                                                                                                                                                                                              | EPHY_V33A         | P           |                | 3.3V I/O power supply for EPHY             |
| Ground pins : 51 pins                                                                                                                                                                                                 |                   |             |                |                                            |
| A1, A4,B2,B4,<br>C2,C3,C4,C5,<br>D2, D3,D4,D5,<br>D6,D7,D8,D9,<br>E2,E4,E5,E6,<br>E7,E8,E9, F1,<br>F2,F3,F4,F6,<br>F7,F8,G6,G7,<br>G8,H6,H7,H8,<br>J6,J7,J8,J9,<br>K9,K10,L10,M10,<br>M11,M12,N10,N13,<br>N14,P10,P14 | GND               | G           |                | Ground pin                                 |
|                                                                                                                                                                                                                       |                   |             | Total: 196pins |                                            |

\*Note:

1. IPD means internal pull-down; IPU means internal pull-up; P means power.
2. While SPI\_CS1 roles as **WATCH DOG RESET**, a pull-high resistance is nessacary.

### 1.3 Pins Sharing Scheme

Some pins are shared with GPIO to provide maximum flexibility for system designers. The RT5350 provides up to 28 GPIO pins. Users can configure SYSCFG and GPIOMODE registers in the System Control block to specify the pin function. Unless it specified explicitly, all the GPIO pins are in input mode after reset.

GPIO share scheme:

| I/O Pad Group | Normal Mode | GPIO Mode |
|---------------|-------------|-----------|
| SPI_CS1       | SPI_CS1     | GPIO#27   |
| SW_PHY_LED    | EPHY_LED4_N | GPIO#26   |
|               | EPHY_LED3_N | GPIO#25   |
|               | EPHY_LED2_N | GPIO#24   |
|               | EPHY_LED1_N | GPIO#23   |
|               | EPHY_LED0_N | GPIO#22   |
| JTAG          | JTAG_TRST_N | GPIO#21   |
|               | JTAG_TCLK   | GPIO#20   |

|       |          |         |
|-------|----------|---------|
|       | JTAG_TMS | GPIO#19 |
|       | JTAG_TDI | GPIO#18 |
|       | JTAG_TDO | GPIO#17 |
| UARTL | RXD2     | GPIO#16 |
|       | TXD2     | GPIO#15 |
| UARTF | RIN      | GPIO#14 |
|       | DSR_N    | GPIO#13 |
|       | DCD_N    | GPIO#12 |
|       | DTR_N    | GPIO#11 |
|       | RXD      | GPIO#10 |
|       | CTS_N    | GPIO#9  |
|       | TXD      | GPIO#8  |
|       | RTS_N    | GPIO#7  |
| SPI   | SPI_MISO | GPIO#6  |
|       | SPI_MOSI | GPIO#5  |
|       | SPI_CLK  | GPIO#4  |
|       | SPI_CS0  | GPIO#3  |
| I2C   | I2C_SCLK | GPIO#2  |
|       | I2C_SD   | GPIO#1  |
| GPIO  | GPIO0    | GPIO#0  |

UARTF pin share scheme

| Pin Name | 3'b000 UARTF | 3'b001 PCM, UARTF | 3'b010 PCM, I2S | 3'b011 I2S UARTF | 3'b100 PCM, GPIO | 3'b101 GPIO, UARTF | 3'b110 GPIO I2S | 3'b111 GPIO |
|----------|--------------|-------------------|-----------------|------------------|------------------|--------------------|-----------------|-------------|
| RIN      | RIN          | PCMDTX            | PCMDTX          | RXD              | PCMDTX           | GPIO#14            | GPIO#14         | GPIO#14     |
| DSR_N    | DSR_N        | PCMDRX            | PCMDRX          | CTS_N            | PCMDRX           | GPIO#13            | GPIO#13         | GPIO#13     |
| DCD_N    | DCD_N        | PCMCLK            | PCMCLK          | TXD              | PCMCLK           | GPIO#12            | GPIO#12         | GPIO#12     |
| DTR_N    | DTR_N        | PCMFS             | PCMFS           | RTS_N            | PCMFS            | GPIO#11            | GPIO#11         | GPIO#11     |
| RXD      | RXD          | RXD               | I2SSDI          | I2SSDI           | GPIO#10          | RXD                | I2SSDI          | GPIO#10     |
| CTS_N    | CTS_N        | CTS_N             | I2SSDO          | I2SSDO           | GPIO#9           | CTS_N              | I2SSDO          | GPIO#9      |
| TXD      | TXD          | TXD               | I2SWS           | I2SWS            | GPIO#8           | TXD                | I2SWS           | GPIO#8      |
| RTS_N    | RTS_N        | RTS_N             | I2SCLK          | I2SCLK           | GPIO#7           | RTS_N              | I2SCLK          | GPIO#7      |

PCM/I2S IO direction:

| Pin Name | I/O |
|----------|-----|
| PCMDTX   | O   |
| PCMDRX   | I   |
| PCMCLK   | I/O |
| PCMFS    | I/O |
| I2SSDI   | I   |
| I2SSDO   | O   |
| I2SWS    | I/O |
| I2SCLK   | /O  |

SPI\_CS1 share scheme: (SPI\_CS1\_MODE)

| Pin Name \ | 2'b00   | 2'b01   | 2'b10(default) |
|------------|---------|---------|----------------|
| SPI_CS1    | SPI_CS1 | WDT_RST | GPIO#27        |

MCS1share scheme: (REFCLK0\_IS\_OUT)

| Pin Name \ | 1'b0(default) | 1'b1        |
|------------|---------------|-------------|
| MCS1       | MCS1          | REFCLK0_OUT |

EPHY\_LED pin share scheme: (EPHY\_BT\_GPIO\_MODE)

| Pin Name \  | 2'b00 (default)<br>EPHY_LED | 2'b01<br>GPIO | 2'b10<br>BT_MODE |
|-------------|-----------------------------|---------------|------------------|
| EPHY_LED4_N | EPHY_LED4_N                 | GPIO#26       | BT_ANT           |
| EPHY_LED3_N | EPHY_LED3_N                 | GPIO#25       | BT_WACT          |
| EPHY_LED2_N | EPHY_LED2_N                 | GPIO#24       | BT_FREQ          |
| EPHY_LED1_N | EPHY_LED1_N                 | GPIO#23       | BT_STAT          |
| EPHY_LED0_N | EPHY_LED0_N                 | GPIO#22       | BT_ACT           |

Notes :

1. All given GPIO are 4mA drive capable.
2. The default direction for GPIO pins are input(i.e. tri-state). Except these GPIO pins:
  - The GPIO17~21 shared with the JTAG interface. The default value for JTAG\_GPIO\_MODE is 0.

### 1.4 Boot strapping description

From signal pad:

| Pin Name                        | Boot Strapping Signal Name | Description                                                                                                                                                                                                                                                       |
|---------------------------------|----------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SPI_CLK                         | XTAL_FREQ_HI               | 0: 20MHz(default)<br>1: 40MHz                                                                                                                                                                                                                                     |
| WLAN_LED_N                      | BIGENDIAN                  | 0: LITTLE ENDIAN(default)<br>1: BIG ENDIAN                                                                                                                                                                                                                        |
| EPHY_LED4_N                     | DRAM_FROM_EE               | 0: DRAM configuration from boot strapping.(default)<br>1: DRAM configuration(size/width) from EEPROM                                                                                                                                                              |
| { EPHY_LED3_N,<br>EPHY_LED2_N } | DRAM_SIZE                  | INIC/AP(SDR)<br>0: 2MB/8MB(default)<br>1: 8MB/16MB<br>2: 16MB/32MB, 32MB*2<br>3: 32MB/                                                                                                                                                                            |
| {EPHY_LED1_N,<br>EPHY_LED0_N }  | CPU_CLK_SEL                | CPU clock select<br>0: 360Mhz(default)<br>1: Reserved<br>2: 320Mhz<br>3: 300Mhz                                                                                                                                                                                   |
| { SPI_MOSI ,<br>TXD2,<br>TXD }  | CHIP_MODE[2:0]             | A vector to set chip function/test/debug modes.<br>In non-test/debug operation,<br>0: Normal mode (boot from SPI serial flash)(default)<br>1: iNIC-USB mode<br>2:Reserved<br>3: Reserved<br>4: Reserved<br>5: iNIC-PHY mode<br>6: scan mode<br>7: debug/test mode |

## 2 Maximum Ratings and Operating Conditions (TBD)

### 2.1 Absolute Maximum Ratings

|                                   |                       |
|-----------------------------------|-----------------------|
| Supply Voltage .....              | 3.6V                  |
| Vcc to Vcc Decouple.....          | -0.3 to +0.3V         |
| Input, Output or I/O Voltage..... | GND -0.3V to Vcc+0.3V |

### 2.2 Thermal Information

|                                                                                     |           |
|-------------------------------------------------------------------------------------|-----------|
| Maximum Junction Temperature (Plastic Package) .....                                | 125°C     |
| Maximum Lead Temperature (Soldering 10s).....                                       | 260°C     |
| Thermal characteristics without external heat sink in still air condition           |           |
| Thermal Resistance $\theta_{JA}$ (oC/W) for JEDEC 2L system PCB .....               | 36.4°C /W |
| Thermal Resistance $\theta_{JA}$ (oC/W) for JEDEC 4L system PCB .....               | 26.3°C /W |
| Thermal Resistance $\theta_{JC}$ (oC/W) for JEDEC 2L system PCB .....               | 7.1°C /W  |
| Thermal Resistance $\theta_{JC}$ (oC/W) for JEDEC 4L system PCB .....               | 6.9°C /W  |
| Thermal Characterization parameter $\Psi_{Jt}$ (oC/W) for JEDEC 2L system PCB ..... | 2.4°C /W  |
| Thermal Characterization parameter $\Psi_{Jt}$ (oC/W) for JEDEC 4L system PCB ..... | 1.7°C /W  |

### 2.3 Operating Conditions

|                          |              |
|--------------------------|--------------|
| Temperature Range .....  | -10 to 55°C  |
| Core Supply Voltage..... | 1.2V +/- 5%  |
| I/O Supply Voltage ..... | 3.3V +/- 10% |

### 2.4 Storage Condition

The calculated shelf life in sealed bag is 12 months if stored between 0°C and 40°C at less than 90% relative humidity (RH). After the bag is opened, devices that are subjected to solder reflow or other high temperature processes must be handled in the following manner:

- Mounted within 168-hours of factory conditions < 30°C /60%RH
- Storage humidity needs to maintained at <10% RH
- Baking is necessary if customer expose the component to air over 168 hrs, backing condition: 125°C / 8hrs

### 2.5 External Xtal Specification

|                        |                 |
|------------------------|-----------------|
| Frequency .....        | 20MHz/40MHz     |
| Frequency offset ..... | +/-20 ppm       |
| VIH/VIL .....          | Vcc-0.3V / 0.3V |
| Duty Cycle .....       | 45%~55%         |

### 2.6 DC Electrical Characteristics

| Parameters               | Sym   | Conditions | Min  | Typ    | Max  | Unit |
|--------------------------|-------|------------|------|--------|------|------|
| 3.3V Supply Voltage      | Vcc33 |            | 3.0  | 3.3    | 3.6  | V    |
| 1.2V Supply Voltage      | Vcc12 |            | 1.14 | 1.2    | 1.26 | V    |
| 3.3V Current Consumption | Icc33 |            |      | 217 mA |      | mA   |
| 1.5V Current Consumption | Icc12 |            |      | 656 mA |      | mA   |

|                                                    |       |  |  |        |  |    |
|----------------------------------------------------|-------|--|--|--------|--|----|
| 2.0V Current Consumption (@transformer center tap) | Icc20 |  |  | 514 mA |  | mA |
|----------------------------------------------------|-------|--|--|--------|--|----|

## 2.7 AC Electrical Characteristics

### 2.7.1 SDRAM Interface

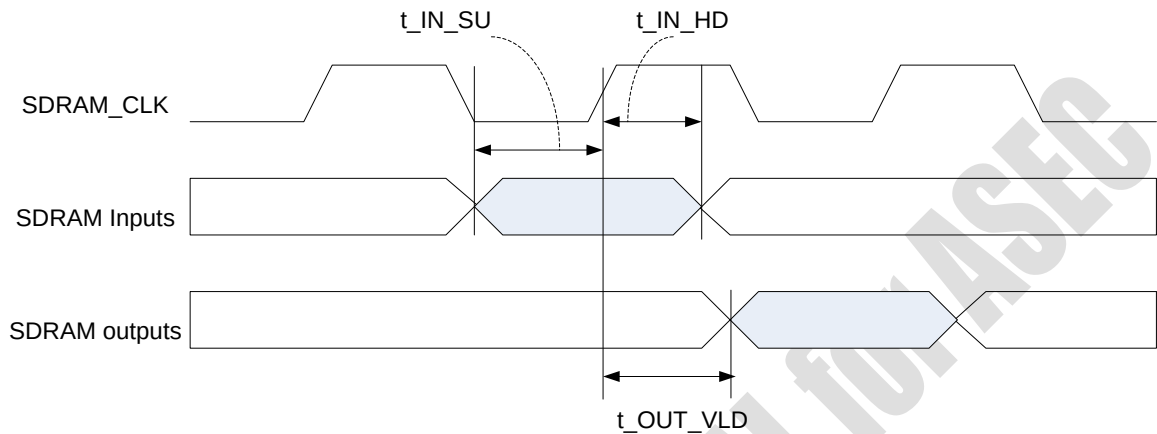


Fig. 2-6-1 SDRAM Interface

| Symbol         | Description                                                   | Min | Max | Unit | Remark            |
|----------------|---------------------------------------------------------------|-----|-----|------|-------------------|
| $t_{IN\_SU}$   | Setup time for Input signals (e.g. MD*)                       | 1.5 | -   | ns   |                   |
| $t_{IN\_HD}$   | Hold time for input signals                                   | 1.7 | -   | ns   |                   |
| $t_{OUT\_VLD}$ | SDRAM_CLK to output signals (MA*, MD*, SDRAM_RAS_N,...) valid | 0.8 | 5   | ns   | output load : 8pF |

### 2.6.5 Power On Sequence

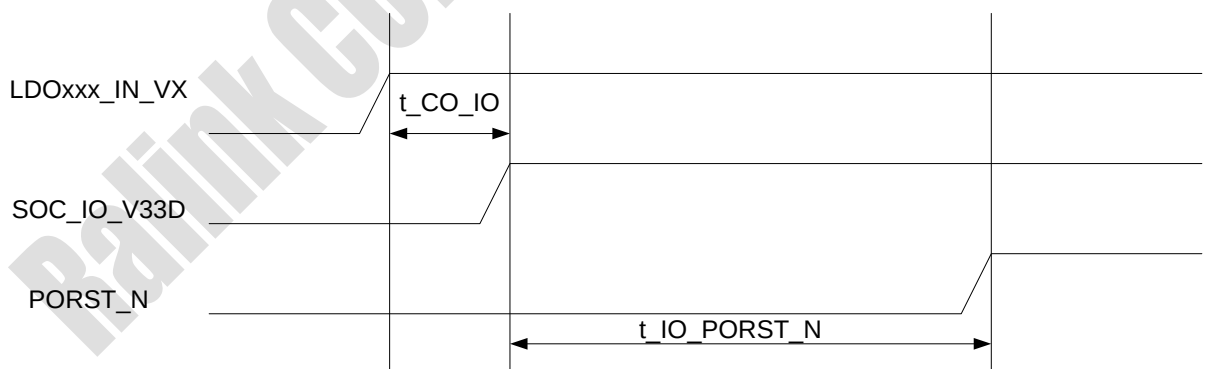


Fig. 2-6-4 Power ON Sequence

| Symbol             | Description                                       | Min | Max | Unit | Remark |
|--------------------|---------------------------------------------------|-----|-----|------|--------|
| $t_{CO\_IO}$       | Time between core power on to I/O power on        | 0   | -   | ms   |        |
| $t_{IO\_PORST\_N}$ | Time between I/O power on to PORST_N de-assertion | 10  | -   | ms   |        |





### 3 Function Description

#### 3.1 Overview

The RT5350 SOC combines Ralink's 802.11n compliant 1T1R MAC/BBP/RF, a high performance 360-MHz MIPS24KEc CPU core and USB controller/PHY, to enable a multitude of high performance, cost-effective 802.11n applications.

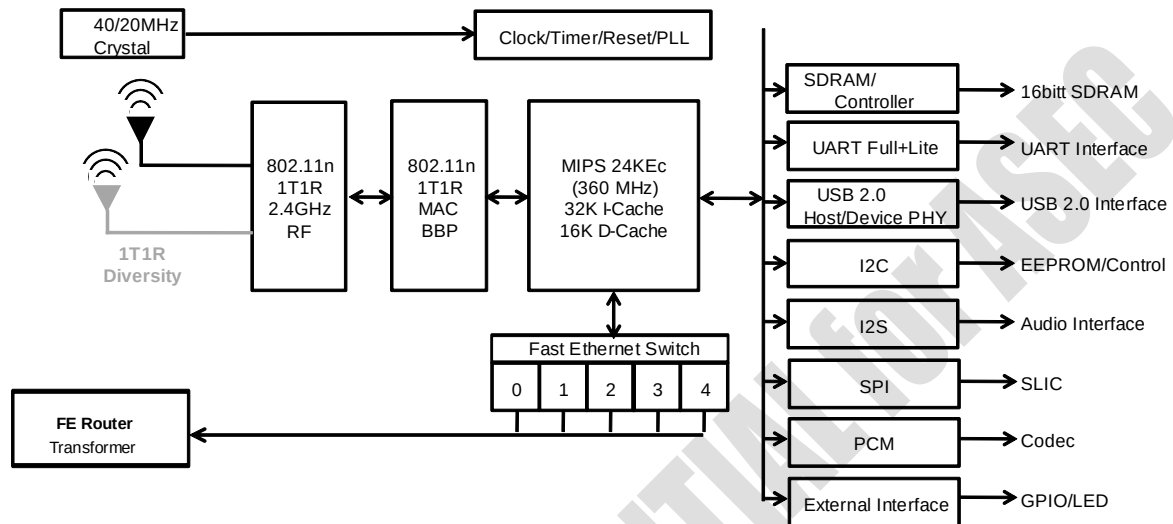


Fig. 3-1-1 RT5350 Block Diagram

There are x bus masters (MIPS 24K, USB Host/Device, and 802.11n MAC/BBP/RF) in the RT5350 SoC on a high performance, low latency Rbus, (Ralink Bus). In addition, the RT5350 SoC supports lower speed peripherals such as UART, GPIO, and SPI via a low speed peripheral bus (Pbus). The SDRAM controller is the only bus slave on the Rbus. It includes an Advanced Memory Scheduler to arbitrate the requests from bus masters, enhancing the performance of memory access intensive tasks.

The RT5350 SoC embeds Ralink's market proven 802.11n 1T1R MAC/BBP/RF to provide a 300Mbps PHY rate on the wireless LAN interface. The MAC design employs a highly efficient DMA engine and hardware data processing accelerators, which free the CPU for user applications. The 802.11n 1T1R MAC/BBP/RF is designed to support standards based features in the area of security, quality of service and international regulation resulting in an enhanced end user experience.

#### 3.2 Memory Map Summary

| Start     |   | End       | Size | Description    |
|-----------|---|-----------|------|----------------|
| 0000.0000 | - | 03FF.FFFF | 64 M | SDRAM 64MB     |
| 0400.0000 | - | 0FFF.FFFF | 192M | Reserved       |
| 1000.0000 | - | 1000.00FF | 256  | SYSCTL         |
| 1000.0100 | - | 1000.01FF | 256  | TIMER          |
| 1000.0200 | - | 1000.02FF | 256  | INTCTL         |
| 1000.0300 | - | 1000.03FF | 256  | MEM_CTRL (SDR) |
| 1000.0400 | - | 1000.04FF | 256  | <<Reserved>>   |

|           |   |           |          |                                                               |
|-----------|---|-----------|----------|---------------------------------------------------------------|
| 1000.0500 | - | 1000.05FF | 256      | UART                                                          |
| 1000.0600 | - | 1000.06FF | 256      | PIO                                                           |
| 1000.0700 | - | 1000.07FF | 256      | Reserved>>                                                    |
| 1000.0800 | - | 1000.08FF | 256      | Reserved>>                                                    |
| 1000.0900 | - | 1000.09FF | 256      | I2C                                                           |
| 1000.0A00 | - | 1000.0AFF | 256      | I2S                                                           |
| 1000.0B00 | - | 1000.0BFF | 256      | SPI                                                           |
| 1000.0C00 | - | 1000.0CFF | 256      | UARTLITE                                                      |
| 1000.0D00 | - | 1000.0DFF | 256      | MIPS CNT                                                      |
| 1000.2000 | - | 1000.27FF | 2 K      | PCM (up to 16 channel)                                        |
| 1000.2800 | - | 1000.2FFF | 2 K      | Generic DMA (up to 64 channel)                                |
| 1000.3000 | - | 1000.37FF | 2 K      | Reserved>>                                                    |
| 1000.3800 | - | 1000.3FFF | 2 K      | Reserved>>                                                    |
| 1000.4000 | - | 100F.FFFF |          | <<Reserved>>                                                  |
| 1010.0000 | - | 1010.FFFF | 64 K     | Frame Engine                                                  |
| 1011.0000 | - | 1011.7FFF | 32 K     | Ethernet Swtich                                               |
| 1011.8000 |   | 1011.BFFF | 16 K     | ROM                                                           |
| 1011.C000 | - | 1011.FFFF | 16 K     | <<Reserved>>                                                  |
| 1012.0000 | - | 1012.7FFF | 16 K     | USB Device                                                    |
| 1012.8000 | - | 1012.FFFF | 16 K     | <<Reserved>>                                                  |
| 1013.0000 | - | 1013.7FFF | 32 K     | <<Reserved>>                                                  |
| 1013.8000 | - | 1013.FFFF | 32 K     | <<Reserved>>                                                  |
| 1014.0000 | - | 1017.FFFF | 256 K    | Reserved>>                                                    |
| 1018.0000 | - | 101B.FFFF | 256 K    | 802.11n MAC/BBP                                               |
| 101C.0000 | - | 101F.FFFF | 256 K    | USB Host                                                      |
| 1020.0000 | - | 1023.FFFF | 256 K    | <<Reserved>>                                                  |
| 1024.0000 | - | 1027.FFFF | 256 K    | <<Reserved>>                                                  |
| 1028.0000 | - | 1BFF.FFFF |          | <<Reserved>>                                                  |
| 1C00.0000 | - | 1C00.3FFF | 16KB ROM | When system is power on,<br>16KB internal boot ROM is mapped. |

Note :

### 3.3 MIPS 24K Processor

#### 3.3.1 Features

- 8-stage pipeline
- 32-bit address paths
- 64-bit data paths to caches and external interface
- MIPS32-Compatible Instruction Set
- Multiply-Accumulate and Multiply-Subtract Instructions (MADD, MADDU, MSUB, MSUBU)
- Targeted Multiply Instruction (MUL)
- Zero/One Detect Instructions (CLZ, CLO)
- Wait Instruction (WAIT)
- Conditional Move Instructions (MOVZ, MOVN)
- Prefetch Instruction (PREF)
- MIPS32 Enhanced Architecture (Release 2) Features
- Vectored interrupts and support for external interrupt controller
- Programmable exception vector base
- Atomic interrupt enable/disable
- GPR shadow registers (optionally, one or three additional shadows can be added to minimize latency for interrupt handlers)
- Bit field manipulation instructions
- MIPS32 Privileged Resource Architecture
- MIPS DSP ASE
- Fractional data types (Q15, Q31)
- Saturating arithmetic
- SIMD instructions operate on 2x16b or 4x8b simultaneously
- 3 additional pairs of accumulator registers
- Programmable Memory Management Unit
- 32 dual-entry JTLB with variable page sizes
- 4-entry ITLB
- 8-entry DTLB
- Optional simple Fixed Mapping Translation (FMT) mechanism
- MIPS16e™ Code Compression
- 16 bit encodings of 32 bit instructions to improve code density
- Special PC-relative instructions for efficient loading of addresses and constants
- SAVE & RESTORE macro instructions for setting up and tearing down stack frames within subroutines
- Improved support for handling 8 and 16 bit datatypes
- Programmable L1 Cache Sizes
- Instruction cache size : 32KB
- Data cache size : 16KB
- 4-Way Set Associative
- Up to 8 outstanding load misses
- Write-back and write-through support
- 32-byte cache line size

### 3.3.2 Block Diagram

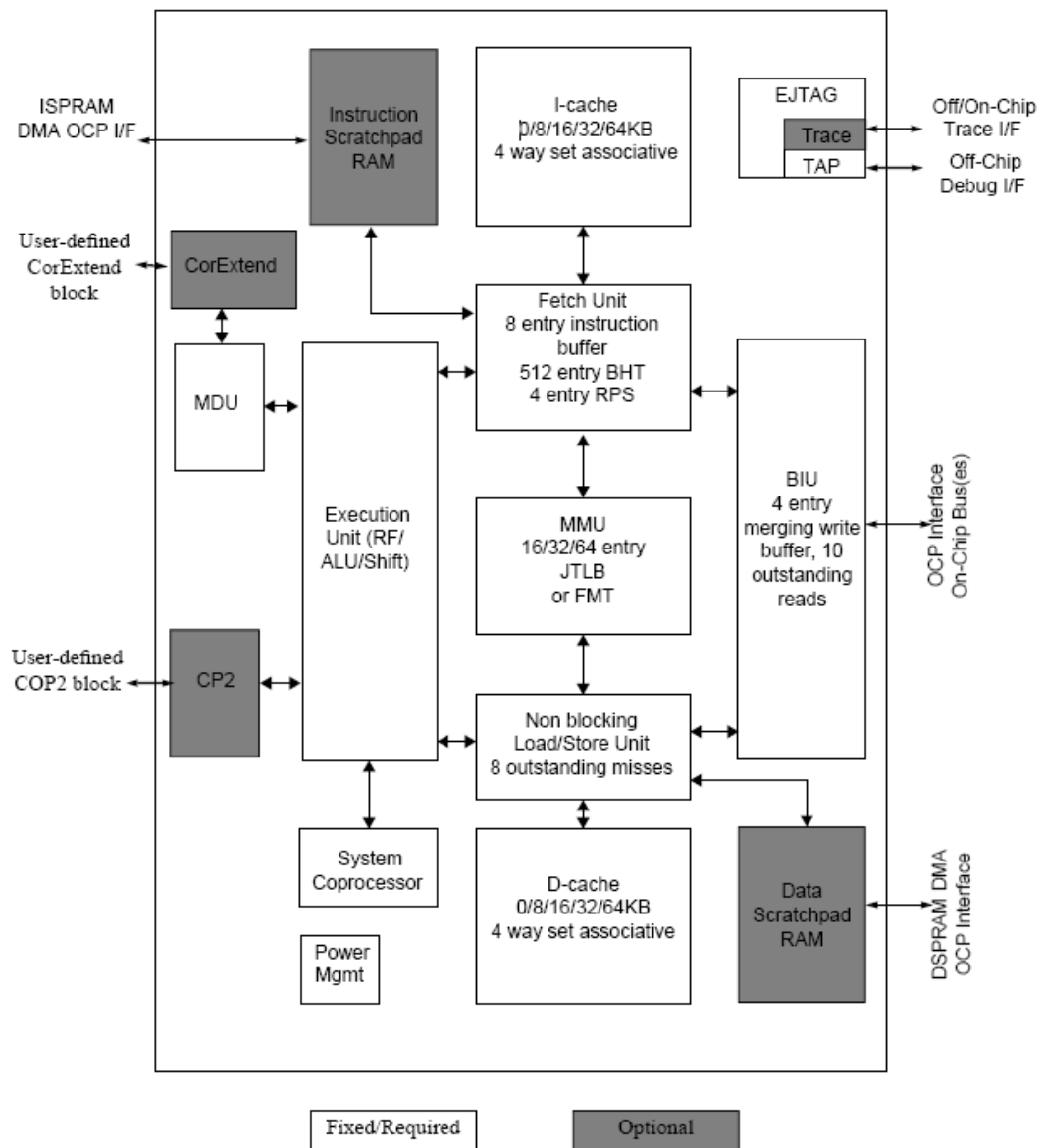


Fig. 3-3-1 MIPS 24KEc Processor Diagram

### 3.3.3 Clock Plan

| CPU  | CPU: BUS(period) | BUS/SDR |
|------|------------------|---------|
| 360M | 1:3              | 120M    |
| 350M | 1:4              | 87.5M   |
| 320M | 1:4              | 80M     |
| 300M | 1:3              | 100M    |

### 3.4 System Control

#### 3.4.1 Features

- Provide read-only chip revision registers
- Provide a window to access boot-strapping signals
- Support memory remapping configurations
- Support software reset to each platform building block
- Provide registers to determine GPIO and other peripheral pin muxing schemes
- Provide some power-on-reset only test registers for software programmers
- Combine miscellaneous registers (such as clock skew control, status register, memo registers,...etc)

#### 3.4.2 Block Diagram

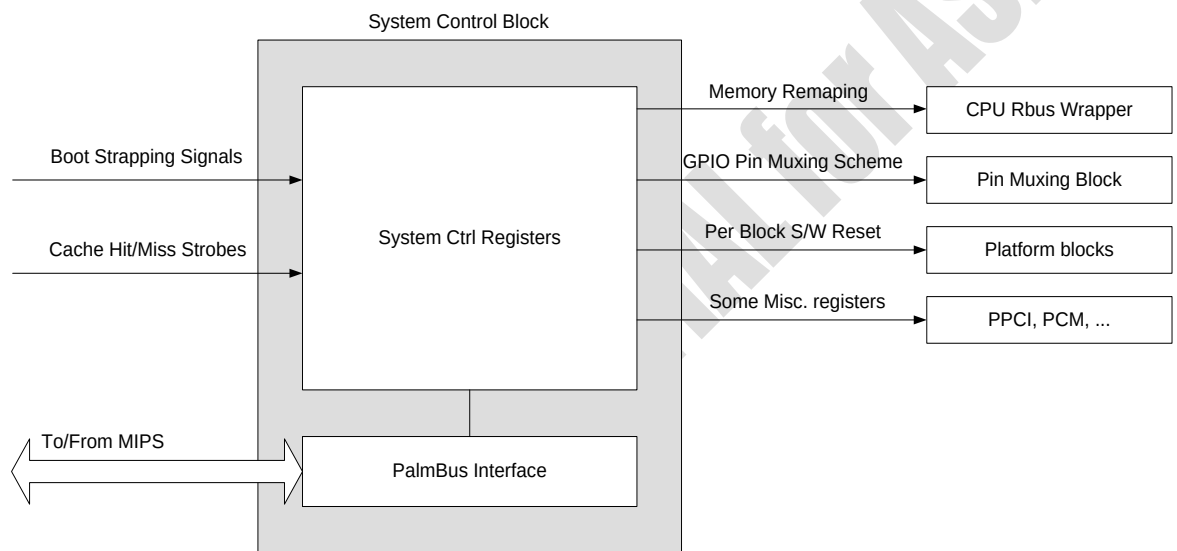


Fig. 3-4-1 System Control Block Diagram

#### 3.4.3 Register Description (base: 0x1000\_0000)

CHIPID0\_3: Chip ID ASCII Character 0-3 (offset: 0x0000)

| Bits  | Type | Name     | Description                                | Initial value |
|-------|------|----------|--------------------------------------------|---------------|
| 31:24 | RO   | CHIP_ID3 | ASCII CHIP Name Identification Character 3 | 0x33          |
| 23:16 | RO   | CHIP_ID2 | ASCII CHIP Name Identification Character 2 | 0x35          |
| 15:8  | RO   | CHIP_ID1 | ASCII CHIP Name Identification Character 1 | 0x54          |
| 7:0   | RO   | CHIP_ID0 | ASCII CHIP Name Identification Character 0 | 0x52          |

CHIPID4\_7: Chip Name ASCII Character 4-7 (offset: 0x0004)

| Bits  | Type | Name     | Description                                | Initial value |
|-------|------|----------|--------------------------------------------|---------------|
| 31:24 | RO   | CHIP_ID7 | ASCII CHIP Name Identification Character 7 | 0x20          |
| 23:16 | RO   | CHIP_ID6 | ASCII CHIP Name Identification Character 6 | 0x20          |
| 15:8  | RO   | CHIP_ID5 | ASCII CHIP Name Identification Character 5 | 0x30          |
| 7:0   | RO   | CHIP_ID4 | ASCII CHIP Name Identification Character 4 | 0x35          |

REVID: Chip Revision Identification (offset: 0x000c)

| Bits  | Type | Name   | Description         | Initial value |
|-------|------|--------|---------------------|---------------|
| 31:12 | -    | -      | Reserved            | -             |
| 11:8  | RO   | VER_ID | Chip Version Number | 0x1           |
| 7:4   | -    | -      | Reserved            | -             |
| 3:0   | RO   | ECO_ID | Chip ECO Number     | 0x1           |

**SYSCFG0: System Configuration Register1 (offset: 0x0010)**

| Bits  | Type | Name           | Description                                                                                                                                                                                                                                    | Initial value |
|-------|------|----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:24 | BS   | TEST_CODE      | Test code<br>Default value is from bootstrap and can be modified by software                                                                                                                                                                   | -             |
| 23:19 | -    | -              | Reserved                                                                                                                                                                                                                                       | -             |
| 20    | BS   | XTAL_SEL       | 0: 20MHz<br>1: 40MHz                                                                                                                                                                                                                           | -             |
| 19    | BS   | BIG_ENDIAN     | 0: LITTLE ENDIAN<br>1: BIG ENDIAN                                                                                                                                                                                                              | -             |
| 18    | BS   | DRAM_FROM_EE   | 0: DRAM configuration from boot strapping.<br>1: DRAM configuration(size/width) from EEPROM                                                                                                                                                    | -             |
| 17    | -    | -              | Reserved                                                                                                                                                                                                                                       | -             |
| 16    | -    | -              | Reserved                                                                                                                                                                                                                                       | -             |
| 15    | -    | -              | Reserved                                                                                                                                                                                                                                       | -             |
| 14:12 | BS   | DRAM_SIZE      | 0: 2MB<br>1: 8MB<br>2: 16MB<br>3: 32MB<br>4: 64MB<br>5-7:Reserved                                                                                                                                                                              | -             |
| 11    | -    | -              | Reserved                                                                                                                                                                                                                                       | -             |
| 10    | BS   | CPU_CLK_SEL[1] |                                                                                                                                                                                                                                                | -             |
| 9     | -    | -              | Reserved                                                                                                                                                                                                                                       | -             |
| 8     | BS   | CPU_CLK_SEL[0] | CPU_CLK_SEL[1:0] : CPU/SYSCLK<br>0 : 360/120 Mhz<br>1 : -Reserved<br>2 : 320/80 Mhz<br>3 : 300/100 Mhz<br>Default value is from bootstrap and the CPU PLL parameter can be modified by software, see CPU_PLL_DYN_CFG.CPU_CLK_SEL (offset:0x48) | -             |
| 7:3   | -    | -              | Reserved                                                                                                                                                                                                                                       | -             |
| 2:0   | BS   | CHIP_MODE      | A vector to set chip function/test/debug modes.<br>In non-test/debug operation,<br>0: Normal mode (AP mode)(default)<br>1: iNIC-USB mode<br>2-4 : Reserved<br>5: iNIC PHY mode<br>6:scan mode<br>7: debug/test mode                            | -             |

**SYSCFG1: System Configuration Register0 (offset: 0x0014)**

| Bits  | Type | Name        | Description                                                                                             | Initial value |
|-------|------|-------------|---------------------------------------------------------------------------------------------------------|---------------|
| 27    | -    | -           | Reserved                                                                                                | -             |
| 26    | RW   | PULL_EN     | PAD pull high/low enable<br>0: disable<br>1: enable                                                     | 0x0           |
| 22:20 | RW   | SDR_PAD_DRV | SDRAM PAD driving strength adjusting<br>SDR_PAD_DRV[2]: for MCLK PAD<br>SDR_PAD_DRV[1] : for MD15-0 PAD | 0x0           |

|       |    |                |                                                                                                                                                                                       |     |
|-------|----|----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|
|       |    |                | SDR_PAD_DRV[0] : for other SDRAM control signal<br>0: low driving<br>1: high driving                                                                                                  |     |
| 19:16 | -  | -              | Reserved                                                                                                                                                                              | -   |
| 13:11 | -  | -              | Reserved                                                                                                                                                                              | -   |
| 10    | RW | USB0_HOST_MODE | 0: Set USB#0 to Device Mode<br>1: Set USB#0 to Host Mode.                                                                                                                             | 0x0 |
| 9     | RW | USB_ISO_EN     | USB PHY Isolation enable<br>In USB less application, the UPHY_VDDL_V12D and UPHY_VDDA_V33A can be tie to GND to save UPHY power.<br>In this application, set this bit to 1 to isolate | 0x0 |
| 3:1   | -  | -              | Reserved                                                                                                                                                                              | -   |
| 0     | -  | -              | Reserved                                                                                                                                                                              | -   |

TESTSTAT: Firmware Test Status Register (offset: 0x0018)

| Bits | Type | Name     | Description                                                                     | Initial value |
|------|------|----------|---------------------------------------------------------------------------------|---------------|
| 31:0 | RW   | TSETSTAT | Firmware Test Status<br>Note : This register is reseted only by power on reset. | 0x0           |

TESTSTAT2: Firmware Test Status Register 2 (offset: 0x001c)

| Bits | Type | Name      | Description                                                                       | Initial value |
|------|------|-----------|-----------------------------------------------------------------------------------|---------------|
| 31:0 | RW   | TSETSTAT2 | Firmware Test Status 2<br>Note : This register is reseted only by power on reset. | 0x0           |

Reserved register (offset: 0x0020)

| Bits | Type | Name | Description | Initial value |
|------|------|------|-------------|---------------|
| 31:0 | -    | -    | Reserved    | 0x0           |

Reserved register (offset: 0x0024)

| Bits | Type | Name | Description | Initial value |
|------|------|------|-------------|---------------|
| 31:0 | -    | -    | Reserved    | 0x0           |

Reserved register (offset: 0x0028)

| Bits | Type | Name | Description | Initial value |
|------|------|------|-------------|---------------|
| 31:0 | -    | -    | Reserved    | 0x0           |

CLKCFG0: Clock Configuration Register 0 (offset: 0x002c)

| Bits  | Type | Name           | Description                                                                                                                                                       | Initial value |
|-------|------|----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:30 | RW   | SDRAM_CLK_SKEW | 0 : zero delay<br>1: delay 200ps<br>2 : delay 400ps<br>3 : delay 600ps                                                                                            | 0x1           |
| 29:23 | -    | -              | Reserved                                                                                                                                                          | -             |
| 22:18 | RW   | INT_CLK_FDIV   | The divisor number of reference clock frequency.<br>Valid value is from 1~31<br><br>Fraction-N clock Frequency =<br>$(INT\_CLK\_FFRAC/INT\_CLK\_FDIV)*PLL\_FREQ$  | 0x08          |
| 17    | -    | -              | Reserved                                                                                                                                                          | -             |
| 16:12 | RW   | INT_CLK_FFRAC  | The fraction number of reference clock frequency.<br>Valid value is from 0~31<br><br>Fraction-N clock Frequency =<br>$(INT\_CLK\_FFRAC/INT\_CLK\_FDIV)*PLL\_FREQ$ | 0x0           |
| 11:9  | RW   | REFCLK0_RATE   | 0: 32K<br>1:12M<br>2:25M                                                                                                                                          | 0x0           |

|     |    |                 |                                                                                                                                                |     |
|-----|----|-----------------|------------------------------------------------------------------------------------------------------------------------------------------------|-----|
|     |    |                 | 3:40M<br>4:48M<br>5: Reserved<br>6: Internal Fraction-N_clk/2<br>7: disable refclk output, MCS1 pin will be input mode if MCS1_AS_REFCLK0 = 1. |     |
| 8   | RW | MCS1_AS_REFCLK0 | To control the MCS1 as REFCLK0 output pin<br>0: MCS1<br>1: Reference clock0 output<br>When this bit is 0, imply cs1 bank is accessible         | 0x0 |
| 7:0 | -  | -               | Reserved                                                                                                                                       | -   |

**CLKCFG1: Clock Configuration Register 1 (offset: 0x0030)**

| Bits  | Type | Name                  | Description                                                                                                                                                         | Initial value |
|-------|------|-----------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31    | -    | -                     | Reserved                                                                                                                                                            | -             |
| 30    | -    | -                     | Reserved                                                                                                                                                            | -             |
| 29    | RW   | SYS_TCK_EN            | System tick enable                                                                                                                                                  | 0x0           |
| 28:23 | -    | -                     | Reserved                                                                                                                                                            | -             |
| 23    | RW   | PDMA_CSR_CLK_GATE_BYP | PDMA csr clock gating bypass control (for USB/WLAN/FE)<br>0: disable bypass HW auto clock gating control for power saving<br>1: Bypass HW auto clock gating control | 0x1           |
| 22    | -    | -                     | Reserved                                                                                                                                                            | -             |
| 21    | -    | -                     | Reserved                                                                                                                                                            | -             |
| 20    | -    | -                     | Reserved                                                                                                                                                            | -             |
| 19    | -    | -                     | Reserved                                                                                                                                                            | -             |
| 18    | RW   | UPHY0_CLK_EN          | 0 : USB PHY0 clock is gated<br>1 : USB PHY0 clock is enabled                                                                                                        | 0x1           |
| 17    | -    | -                     | Reserved                                                                                                                                                            | -             |
| 16    | -    | -                     | Reserved                                                                                                                                                            | -             |
| 15:0  | -    | -                     | Reserved                                                                                                                                                            | -             |

**RSTCTRL: Reset Control Register (offset: 0x0034)**

| Bits  | Type | Name         | Description                                                                         | Initial value |
|-------|------|--------------|-------------------------------------------------------------------------------------|---------------|
| 31:29 | -    | -            | Reserved                                                                            | -             |
| 28    | RW   | MIPS_CNT_RST | Write 1 to this bit will reset mips counter block<br>Write 0 to de-assert reset.    | 0x0           |
| 27    | -    | -            | Reserved                                                                            | -             |
| 26    | -    | -            | Reserved                                                                            | -             |
| 25    | RW   | UDEV_RST     | Write 1 to this bit will reset USB Device block<br>Write 0 to de-assert reset.      | 0x0           |
| 24    | RW   | EPHY_RST     | Write 1 to this bit will reset Ethernet PHY block<br>Write 0 to de-assert reset.    | 0x0           |
| 23    | RW   | ESW_RST      | Write 1 to this bit will reset Ethernet Switch block<br>Write 0 to de-assert reset. | 0x0           |
| 22    | RW   | UHST_RST     | Write 1 to this bit will reset USB Host block<br>Write 0 to de-assert reset.        | 0x0           |
| 21    | RW   | FE_RST       | Write 1 to this bit will reset Frame Engine block<br>Write 0 to de-assert reset.    | 0x0           |
| 20    | RW   | WLAN_RST     | Write 1 to this bit will reset RT2863 block<br>Write 0 to de-assert reset.          | 0x0           |
| 19    | RW   | UARTL_RST    | Write 1 to this bit will reset UART Lite block<br>Write 0 to de-assert reset.       | 0x0           |



|     |     |           |                                                                                          |     |
|-----|-----|-----------|------------------------------------------------------------------------------------------|-----|
| 18  | RW  | SPI       | Write 1 to this bit will reset SPI block<br>Write 0 to de-assert reset.                  | 0x0 |
| 17  | RW  | I2S       | Write 1 to this bit will reset I2S block<br>Write 0 to de-assert reset.                  | 0x0 |
| 16  | RW  | I2C       | Write 1 to this bit will reset I2C block<br>Write 0 to de-assert reset.                  | 0x0 |
| 15  | -   | -         | Reserved                                                                                 | -   |
| 14  | RW  | DMA       | Write 1 to this bit will reset DMA block<br>Write 0 to de-assert reset.                  | 0x0 |
| 13  | RW  | PIO       | Write 1 to this bit will reset PIO block<br>Write 0 to de-assert reset.                  | 0x0 |
| 12  | RW  | UART_RST  | Write 1 to this bit will reset UART block<br>Write 0 to de-assert reset.                 | 0x0 |
| 11  | RW  | PCM_RST   | Write 1 to this bit will reset PCM block<br>Write 0 to de-assert reset.                  | 0x0 |
| 10  | RW  | MC_RST    | Write 1 to this bit will reset Memory Controller block<br>Write 0 to de-assert reset.    | 0x0 |
| 9   | RW  | INTC_RST  | Write 1 to this bit will reset Interrupt Controller block<br>Write 0 to de-assert reset. | 0x0 |
| 8   | RW  | TIMER_RST | Write 1 to this bit will reset Timer block<br>Write 0 to de-assert reset.                | 0x0 |
| 7:1 | -   | Reserved  |                                                                                          | -   |
| 0   | W1C | SYS_RST   | Write 1 to this bit will reset Whole SoC                                                 | 0x0 |

RSTSTAT: Reset Status Register (offset: 0x0038)

| Bits | Type | Name     | Description                                                                                                                                                                                                                                               | Initial value |
|------|------|----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:4 | -    | -        | Reserved                                                                                                                                                                                                                                                  | 0x0           |
| 3    | RC   | SWCPURST | Software CPU reset occurred<br>This bit will be set if software reset the CPU by writing to the RSTCPU bit in RSTCTL. Writing a '1' will clear this bit. Writing a '0' has not effect.<br><br>Note : This register is reseted only by power on reset.     | 0x0           |
| 2    | RC   | SWSYSRST | Software system reset occurred<br>This bit will be set if software reset the chip by writing to the RSTSYS bit in RSTCTL. Writing a '1' will clear this bit. Writing a '0' has not effect.<br><br>Note : This register is reseted only by power on reset. | 0x0           |
| 1    | RC   | WDRST    | Watchdog reset occurred<br>This bit will be set if the watchdog timer reset the chip. Writing a '1' will clear this bit. Writing a '0' has not effect.<br><br>Note : This register is reseted only by power on reset.                                     | 0x0           |
| 0    | -    | -        | Reserved                                                                                                                                                                                                                                                  | 0x0           |

CPU\_SYS\_CLKCFG: CPU and SYS clock control(offset: 0x003c)

| Bits  | Type | Name          | Description                                                                                                                                       | Initial value |
|-------|------|---------------|---------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31    | -    | -             | Reserved                                                                                                                                          | 0x0           |
| 30:24 | RW   | OCP_FDIV      | The divider number of OCP(bus) clock frequency<br>It is referred when CPU_OCP_RATIO is set as "3'b100"<br>OCP bus clock will be CPU_FREQ/OCP_FDIV | 0x03          |
| 23:20 | -    | -             | Reserved                                                                                                                                          | -             |
| 19:16 | RW   | CPU_OCP_RATIO | The ratio is system bus frequency compare with CPU frequency.                                                                                     | BS            |

|       |    |           | Value                                                                                                                                                                                                                                                                                                                                                        | Ratio(CPU : SYS) |      |
|-------|----|-----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------|------|
|       |    |           | 4'b0000                                                                                                                                                                                                                                                                                                                                                      | Reserved         |      |
|       |    |           | 4'b0001                                                                                                                                                                                                                                                                                                                                                      | Reserved         |      |
|       |    |           | 4'b0010                                                                                                                                                                                                                                                                                                                                                      | 2 : 1            |      |
|       |    |           | 4'b0011                                                                                                                                                                                                                                                                                                                                                      | Reserved         |      |
|       |    |           | 4'b0100                                                                                                                                                                                                                                                                                                                                                      | 3 : 1            |      |
|       |    |           | 4'b0101                                                                                                                                                                                                                                                                                                                                                      | Reserved         |      |
|       |    |           | 4'b0110                                                                                                                                                                                                                                                                                                                                                      | 4 : 1            |      |
|       |    |           | 4'b0111                                                                                                                                                                                                                                                                                                                                                      | 5 : 1            |      |
|       |    |           | 4'b1000                                                                                                                                                                                                                                                                                                                                                      | 10 : 1           |      |
|       |    |           | Note: If chip run with USB OHCI mode, the OCP frequency can't lower than 12MHz. It means that $PLL\_FREQ * (CPU\_FFRAC / CPU\_FDIV) / (CPU\_OCP\_RATIO + 1) \geq 12MHz$                                                                                                                                                                                      |                  |      |
| 15:13 | -  | -         | Reserved                                                                                                                                                                                                                                                                                                                                                     |                  | 0x0  |
| 12:8  | RW | CPU_FDIV  | The divider number of CPU frequency<br>The value must larger than or equal CPU_FFRAC.<br>Valid value is from (1~31)<br><br>CPU Frequency = $(CPU\_FFRAC / CPU\_FDIV) * PLL\_FREQ$<br>Note: If chip run with USB OHCI mode, the OCP frequency can't lower than 12MHz. It means that $PLL\_FREQ * (CPU\_FFRAC / CPU\_FDIV) / (CPU\_OCP\_RATIO + 1) \geq 12MHz$ |                  | 0x01 |
| 7:5   | -  | -         | Reserved                                                                                                                                                                                                                                                                                                                                                     |                  | 0x0  |
| 4:0   | RW | CPU_FFRAC | The fraction number of CPU frequency.<br>Valid value is from 0~31<br><br>CPU Frequency = $(CPU\_FFRAC / CPU\_FDIV) * PLL\_FREQ$<br>Note: If chip run with USB OHCI mode, the OCP frequency can't lower than 12MHz. It means that $PLL\_FREQ * (CPU\_FFRAC / CPU\_FDIV) / (CPU\_OCP\_RATIO + 1) \geq 12MHz$                                                   |                  | 0x01 |

CLK\_LUT\_CFG: CPU and SYS clock auto control(offset: 0x0040)

| Bits  | Type | Name              | Description                                                                                                                                                                                                                                                                                              | Initial value |
|-------|------|-------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31    | RW   | CLK_LUT_EN        | Clock Lookup table enable<br>0: Disable<br>1: Enable                                                                                                                                                                                                                                                     | 0x0           |
| 30:23 | RW   | LUT_CNT           | The counter is used to count the period of DRAM idle status. When the counter down count to zero, the cpu clock will be automatically change to specified frequency ( $360M * CPU\_AUTO\_FFRAC / CPU\_AUTO\_FDIV$ ).<br>The count period is $((AUTO\_CNT + 1) * 16 - 1)us$ (Range is from 15us ~ 4095us) | 0x0           |
| 22:16 | RW   | LUT_OCP_FDIV      | The divider number of OCP(bus) clock frequency in auto mode.<br>It is referred when CPU_AUTO_OCP_RATIO is set as "3'b100"<br>OCP bus clock will be $CPU\_FREQ / AUTO\_OCP\_FDIV$ in auto enable mode                                                                                                     | 0x03          |
| 15:13 | RW   | CPU_LUT_OCP_RATIO | The ratio is system bus frequency compare with CPU frequency.<br>3'b000: 1 : 1 (CPU : SYS)                                                                                                                                                                                                               | 0x2           |

|      |    |               |                                                                                                                                                                                                                                                                                                                                                              |      |
|------|----|---------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|
|      |    |               | 3'b001: 1 : 2 (CPU : SYS)<br>3'b010: 1 : 3 (CPU : SYS)<br>3'b011: 1 : 4 (CPU : SYS)<br>3'b100: 1: AUTO_OCP_FDIV (Soft setting)<br>Note: If chip run with USB OHCI mode, the OCP frequency can't lower than 12MHz. It means that $PLL\_FREQ * (CPU\_FFRAC / CPU\_FDIV) / (CPU\_OCP\_RATIO + 1) \geq 12MHz$                                                    |      |
| 12:8 | RW | CPU_LUT_FDIV  | The divider number of CPU frequency<br>The value must larger than or equal CPU_FFRAC.<br>Valid value is from (1~31)<br><br>CPU Frequency = $(CPU\_FFRAC / CPU\_FDIV) * PLL\_FREQ$<br>Note: If chip run with USB OHCI mode, the OCP frequency can't lower than 12MHz. It means that $PLL\_FREQ * (CPU\_FFRAC / CPU\_FDIV) / (CPU\_OCP\_RATIO + 1) \geq 12MHz$ | 0x05 |
| 7:5  | RW | LUT_FREQ_SCAL | The lookup table of Clock frequency scaling<br>3'b100~3'b111: Reserved<br>3'b011: Sleep and RP will introduce the clock frequency scaling down<br>3'b010: Sleep will introduce the clock frequency scaling down<br>3'b001: RP will introduce the clock frequency scaling down<br>3'b000: None will introduce the clock frequency scaling down                | 0x0  |
| 4:0  | RW | CPU_LUT_FFRAC | The fraction number of CPU frequency.<br>Valid value is from 0~31<br><br>CPU Frequency = $(CPU\_FFRAC / CPU\_FDIV) * PLL\_FREQ$<br>Note: If chip run with USB OHCI mode, the OCP frequency can't lower than 12MHz. It means that $PLL\_FREQ * (CPU\_FFRAC / CPU\_FDIV) / (CPU\_OCP\_RATIO + 1) \geq 12MHz$                                                   | 0x01 |

CPU\_CLK\_AUTO\_CFG: CPU clock auto dynamic control(offset: 0x0044)

| Bits  | Type | Name            | Description                                                                                                                                                                                                                                                                                          | Initial value |
|-------|------|-----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31    | RW   | CPU_AUTO_CLK_EN | CPU auto clock enable<br>0: disable<br>1: enable<br><br><i>Note: After change this control from enable to disable, software need to use CPU_SYS_CLKCFG(0x3C) register to reconfig the CPU back to 1:1 PLL frequency. Or the system will run at certain frequency which depend on system loading.</i> | 0x0           |
| 30:21 | -    | -               | Reserved                                                                                                                                                                                                                                                                                             | -             |
| 20:16 | RW   | CLK_ADJ_STEP    | The step of cpu clock adjustment. (2~31)<br>The one step value is $(PLL\_CLK / CLK\_ADJ\_STEP)$                                                                                                                                                                                                      | 0x1f          |
| 15:12 | -    | -               | Reserved                                                                                                                                                                                                                                                                                             | -             |
| 11:8  | RW   | UTL_PERIOD      | The unit is system tick. The calculation of CPU active utilization is during the period of $(UTL\_PERIOD + 1) * system\_tick\_time$ .<br>Ex. If the system tick is 4ms, the default CPU active utilization will be calculated during period of 8ms( $2 * 4ms$ )                                      | 0x1           |

|     |    |             |                                                                                                                                                                                               |     |
|-----|----|-------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|
| 7:6 | -  | -           | Reserved                                                                                                                                                                                      | -   |
| 5:4 | RW | UTL_HI_MARK | Set the high mark of CPU active utilization. When the CPU active utilization is higher than specified value, the CPU freq will be speeded up.<br>00: 50%<br>01: 62.5%<br>10: 75%<br>11: 87.5% | 0x1 |
| 3:2 | -  | -           | Reserved                                                                                                                                                                                      | -   |
| 1:0 | RW | UTL_LO_MARK | Set the low mark of CPU active utilization. When the CPU active utilization is lower than specified value, the CPU freq will be slowed down.<br>00: 12.5%<br>01: 25%<br>10: 37.5%<br>11: 50%  | 0x2 |

CPU\_PLL\_DYN\_CFG: CPU PLL Dynamic Configuration (offset: 0x0048)

| Bits  | Type | Name           | Description                                                                                                                | Initial value |
|-------|------|----------------|----------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:25 | RW   | CPLL_F         | CPLL feedback divider control                                                                                              | BS            |
| 24:20 | RW   | CPLL_R         | CPLL divider control                                                                                                       | BS            |
| 19:18 | RW   | CPLL_OD        | CPLL output divider control                                                                                                | BS            |
| 17:16 | RW   | CPLL_BS        | CPLL Output band control                                                                                                   | BS            |
| 15:10 | -    | -              | Reserved                                                                                                                   | -             |
| 9     | -    | -              | Reserved                                                                                                                   | -             |
| 8     | RW   | CPLL_NEW_PARMS | CPLL use new parameters (CPLL_F, CPLL_R, CPLL_OD, CPLL_BS).                                                                | 0x0           |
| 7:3   | -    | -              | Reserved                                                                                                                   | -             |
| 2     | RW   | CPLL_PD        | Set CPU PLL into Power down mode                                                                                           | 0x0           |
| 1     | RW   | CPU_CLK_240M   | Select CPU source clock from temporary 240Mhz clock<br>1: CPU clock run in 240Mhz<br>0: CPU clock according to CPU_CLK_SEL | 0x0           |
| 0     | RO   | CPLL_LD        | Read the CPLL lockdown status                                                                                              | 0x1           |

RF\_RX\_SD\_CFG: RF RX signal detection power saving control(offset: 0x0058)

| Bits  | Type | Name        | Description                                                                                                                                                                                              | Initial value |
|-------|------|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31    | RW   | RX_SD_EN    | Enable the RX_SD_ACT signal control to RF<br>0: disable<br>1: enable                                                                                                                                     | 0x0           |
| 30:15 | -    | -           | Reserved                                                                                                                                                                                                 | -             |
| 14:8  | RW   | ACT_TIME    | The active time period control for RX_SD_ACT. (range is 1~128us)<br>The period formula is (ACT_TIME + 1) * 1us<br>EX: ACT_TIME is "2", the RX_SD_ACT will active for (2+1)*1us = 3us                     | 0x02          |
| 7     | -    | -           | Reserved                                                                                                                                                                                                 | -             |
| 6:0   | RW   | NONACT_TIME | The non active time period control for RX_SD_ACT. (range is 1~128us)<br>The period formula is (NONACT_TIME + 1) * 1us<br>EX: NONACT_TIME is "127", the RX_SD_ACT will not active for (127+1)*1us = 128us | 0x7f          |

GPIO\_MODE: GPIO Purpose Select (offset: 0x0060)

| Bits  | Type | Name              | Description                                                                                                                                             | Initial value |
|-------|------|-------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:23 | -    | -                 | Reserved                                                                                                                                                | -             |
| 22:21 | RW   | SPI_CS1_MODE      | SPI_CS1 as watch dog timeout<br>2'b00: SPI_CS1<br>2'b01: Watch dog reset output (active low for 3 system clocks)<br>2'b10: GPIO mode<br>2'b11: Reserved | 0x2           |
| 20:16 | -    | -                 | Reserved                                                                                                                                                | -             |
| 15:14 | RW   | EPHY_BT_GPIO_MODE | 00: Normal Mode, as EPHY LED0-4<br>01: GPIO Mode<br>10: BT Mode<br>11: Reserved                                                                         | 0x0           |
| 13:7  | -    | -                 | Reserved                                                                                                                                                | -             |
| 6     | RW   | JTAG_GPIO_MODE    | 0: Normal Mode<br>1: GPIO Mode                                                                                                                          | 0x0           |
| 5     | RW   | UARTL_GPIO_MODE   | 0: Normal Mode<br>1: GPIO Mode                                                                                                                          | 0x1           |
| 4:2   | RW   | UARTF_SHARE_MODE  | UARTF Full interface is shared with PCM, I2S, GPIO.<br>The detailed UARTF Mode Pin Sharing is shown in previous session.                                | 0x7           |
| 1     | RW   | SPI_GPIO_MODE     | 0: Normal Mode<br>1: GPIO Mode                                                                                                                          | 0x1           |
| 0     | RW   | I2C_GPIO_MODE     | 0: Normal Mode<br>1: GPIO Mode                                                                                                                          | 0x1           |

PMU: (offset: 0x0088)

| Bits  | Type | Name     | Description                                                                                      | Initial value |
|-------|------|----------|--------------------------------------------------------------------------------------------------|---------------|
| 31:23 | -    | -        | Reserved                                                                                         | -             |
| 22    | RW   | a_undisb | under voltage monitor function (default : 1)                                                     | 0x1           |
| 21:20 | -    | -        | Reserved                                                                                         | -             |
| 19:12 | RW   | a_vtune  | Programmable output voltage level (default: <10100100>)<br>MSB is read only and be fixed to 1'b1 | 0xc9          |
| 11    | -    | -        | Reserved                                                                                         | -             |
| 10:8  | RW   | a_dly    | Output power MOSFET dead zone control (default : <011>).                                         | 0x3           |
| 7:4   | RW   | a_drven  | Output power MOSFET driving control (default : <0100>).                                          | 0x4           |
| 3:0   | -    | -        | Reserved                                                                                         | -             |

PMU1: (offset: 0x008c)

| Bits  | Type | Name           | Description                                                         | Initial value |
|-------|------|----------------|---------------------------------------------------------------------|---------------|
| 31:24 | -    | -              | Reserved                                                            | -             |
| 23:16 | RW   | a_opt_ldolevel | Ido output level selection<br>MSB is read only and be fixed to 1'b1 | 0xd6          |
| 15:8  | RW   | a_dig_ldolevel | Ido output level selection<br>MSB is read only and be fixed to 1'b1 | 0x9b          |
| 7:0   | -    | -              | Reserved                                                            | -             |

(The remainder of this page is left blank intentionally)

**3.5 Timer(TBD)(Should be update from RT3680 by Leon)****3.5.1 Features**

- Independent clock pre-scale for each timer
- Independent interrupts for each timer
- Two General-purpose timers
- Periodic mode
- Free-running mode
- Time-out mode
- Second timer may be used as watchdog timer
- Watchdog timer resets system on time-out
- Timer Modes

**Periodic:**

In periodic mode, the timer counts down to zero from the load value. An interrupt is generated when the count is zero. After reaching zero, the load value is reloaded into the timer and the timer counts down again. A load value of zero disables the timer.

**Timeout:**

In timeout mode, the timer counts down to zero from the load value. An interrupt is generated when the count is zero. In this mode, the ENABLE bit is reset when the timer reaches zero, stopping the counter. After reaching zero, the load value is reloaded into the timer. A load value of zero disables the timer.

**Free-running:**

In free-running mode, the timer counts down to zero from FFFFh. An interrupt is generated when the count is zero. After reaching zero, FFFFh is reloaded into the timer. This mode is identical to the periodic mode with a load value of 65535. Though it is worth noting that if firmware writes to the load value register in this mode, the timer will still load that value even though that value will be ignored thereafter. Also note that when the timer is first enabled, it will begin counting down from its current value, not necessarily FFFFh.

**Watchdog:**

In watchdog mode, the timer counts down to zero from the load value. If the load value is not reloaded or the timer is not disabled before the count is zero, the chip will be reset. When this occurs, every register in the chip is reset except the watchdog reset status bit WDRST in the RSTSTAT register in the system control block; it remains set to alert firmware of the timeout event when it re-executes its bootstrap.

### 3.5.2 Block Diagram

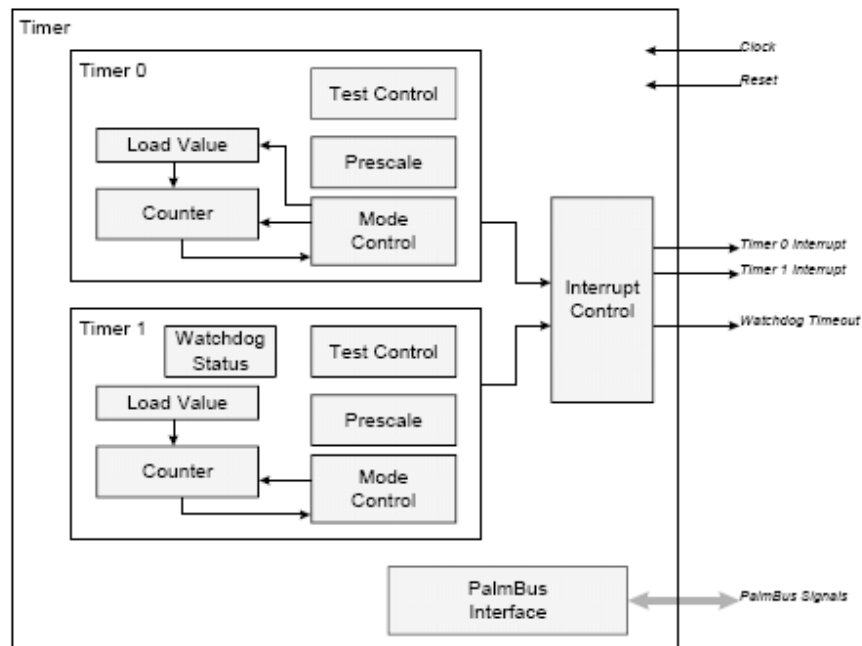


Fig. 3-5-1 Timer Block Diagram

### 3.5.3 Register Description (base: 0x1000\_0100)

TMRSTAT: Timer Status Register (offset: 0x0000)

| Bits | Type | Name    | Description                                                                                                                                                                                                                                                             | Initial value |
|------|------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:6 | -    | -       | Reserved                                                                                                                                                                                                                                                                | -             |
| 5    | WO   | TMR1RST | <p>Timer 1 Reset</p> <p>Writing a '1' to this bit will reset the Timer 1 to 0xFFFF if in free-running mode, or the value specified in the TMR1LOAD register in all other modes.</p> <p>Writing a '0' to this bit has no effect. Reading this bit will return a '0'.</p> | 0x0           |
| 4    | WO   | TMR0RST | <p>Timer 0 Reset</p> <p>Writing a '1' to this bit will reset Timer 0 to 0xFFFF if in free-running mode, or the value specified in the TMR0LOAD register in all other modes.</p> <p>Writing a '0' to this bit has no effect. Reading this bit will return a '0'.</p>     | 0x0           |
| 3:2  | -    | -       | Reserved                                                                                                                                                                                                                                                                | -             |
| 1    | W1C  | TMR1INT | <p>Timer 1 Interrupt Status</p> <p>This bit is set if Timer 1 has expired. The Timer 1 interrupt to the processor is set when this bit is '1'. Writing a '1' to this bit will clear the interrupt. Writing a '0' has no effect.</p>                                     | 0x0           |
| 0    | W1C  | TMR0INT | <p>Timer 0 Interrupt Status</p> <p>This bit is set if Timer 0 has expired. The Timer 0 interrupt to the processor is set when this bit is '1'. Writing a '1' to this bit will clear the interrupt. Writing a '0' has no effect.</p>                                     | 0x0           |

TMR0LOAD: Timer 0 Load Value (offset: 0x0010)

| Bits  | Type | Name | Description | Initial value |
|-------|------|------|-------------|---------------|
| 31:16 | -    | -    | Reserved    | -             |



|      |    |         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |     |
|------|----|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|
| 15:0 | RW | TMRLOAD | <p>Timer Load Value</p> <p>This register contains the load value for the timer. In all modes, this value is loaded into the timer counter when this register is written. In all modes except free-running mode, this value is reloaded into the timer counter after the timer counter reaches 0. It may be updated at any time; the new value will be written to the counter immediately. Writing a load value of 0 will disable the timer, except in free-running mode.</p> | 0x0 |
|------|----|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|

TMR0VAL: Timer 0 Counter Value (offset: 0x0014)

| Bits  | Type | Name   | Description                                                                                                                                  | Initial value |
|-------|------|--------|----------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:16 | -    | -      | Reserved                                                                                                                                     | -             |
| 15:0  | RO   | TMRVAL | <p>Timer Counter Value</p> <p>This register contains the current value of the timer. During functional operation, writes have no effect.</p> | 0xffff        |

TMR0CTL: Timer 0 Control (offset: 0x0018)

| Bits  | Type                  | Name     | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | Initial value |                       |   |              |   |                  |   |                  |   |                   |   |   |   |                      |    |                      |    |  |     |
|-------|-----------------------|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|-----------------------|---|--------------|---|------------------|---|------------------|---|-------------------|---|---|---|----------------------|----|----------------------|----|--|-----|
| 31:16 | -                     | -        | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | -             |                       |   |              |   |                  |   |                  |   |                   |   |   |   |                      |    |                      |    |  |     |
| 15    | RW                    | TESTEN   | Reserved for Test<br>This bit should be written with a zero                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | 0x0           |                       |   |              |   |                  |   |                  |   |                   |   |   |   |                      |    |                      |    |  |     |
| 14:8  | -                     | -        | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | -             |                       |   |              |   |                  |   |                  |   |                   |   |   |   |                      |    |                      |    |  |     |
| 7     | RW                    | ENABLE   | Timer Enable<br>0: Disable the timer. The timer will stop counting and will retain its current value.<br>1: Enable the timer. The timer will begin counting from its current value.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | 0x0           |                       |   |              |   |                  |   |                  |   |                   |   |   |   |                      |    |                      |    |  |     |
| 6     | -                     | -        | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | -             |                       |   |              |   |                  |   |                  |   |                   |   |   |   |                      |    |                      |    |  |     |
| 5:4   | RW                    | MODE     | Timer Mode<br>0: Free-running<br>1: Periodic<br>2: Time-out<br>3: Time-out                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | 0x0           |                       |   |              |   |                  |   |                  |   |                   |   |   |   |                      |    |                      |    |  |     |
| 3:0   | RW                    | PRESCALE | Timer Clock Pre-scale<br>These bits are used to scale the timer clock in order to achieve higher resolution or longer timer periods. Their definitions are below. <table><tr><th>Value</th><th>Timer Clock Frequency</th></tr><tr><td>0</td><td>System clock</td></tr><tr><td>1</td><td>System clock / 4</td></tr><tr><td>2</td><td>System clock / 8</td></tr><tr><td>3</td><td>System clock / 16</td></tr><tr><td>.</td><td>.</td></tr><tr><td>.</td><td>System clock / 32768</td></tr><tr><td>14</td><td>System clock / 65536</td></tr><tr><td>15</td><td></td></tr></table> <b>Note:</b> The pre-scale value should not be changed unless the timer is disabled. | Value         | Timer Clock Frequency | 0 | System clock | 1 | System clock / 4 | 2 | System clock / 8 | 3 | System clock / 16 | . | . | . | System clock / 32768 | 14 | System clock / 65536 | 15 |  | 0x0 |
| Value | Timer Clock Frequency |          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |               |                       |   |              |   |                  |   |                  |   |                   |   |   |   |                      |    |                      |    |  |     |
| 0     | System clock          |          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |               |                       |   |              |   |                  |   |                  |   |                   |   |   |   |                      |    |                      |    |  |     |
| 1     | System clock / 4      |          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |               |                       |   |              |   |                  |   |                  |   |                   |   |   |   |                      |    |                      |    |  |     |
| 2     | System clock / 8      |          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |               |                       |   |              |   |                  |   |                  |   |                   |   |   |   |                      |    |                      |    |  |     |
| 3     | System clock / 16     |          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |               |                       |   |              |   |                  |   |                  |   |                   |   |   |   |                      |    |                      |    |  |     |
| .     | .                     |          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |               |                       |   |              |   |                  |   |                  |   |                   |   |   |   |                      |    |                      |    |  |     |
| .     | System clock / 32768  |          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |               |                       |   |              |   |                  |   |                  |   |                   |   |   |   |                      |    |                      |    |  |     |
| 14    | System clock / 65536  |          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |               |                       |   |              |   |                  |   |                  |   |                   |   |   |   |                      |    |                      |    |  |     |
| 15    |                       |          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |               |                       |   |              |   |                  |   |                  |   |                   |   |   |   |                      |    |                      |    |  |     |

TMR1LOAD: Timer 1 Load Value (offset: 0x0020)

| Bits  | Type | Name    | Description                                                                                | Initial value |
|-------|------|---------|--------------------------------------------------------------------------------------------|---------------|
| 31:16 | -    | -       | Reserved                                                                                   | -             |
| 15:0  | RW   | TMRLOAD | <p>Timer Load Value</p> <p>This register contains the load value for the timer. In all</p> | 0x0           |

|  |  |  |                                                                                                                                                                                                                                                                                                                                                                                   |  |
|--|--|--|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|
|  |  |  | modes, this value is loaded into the timer counter when this register is written. In all modes except free-running mode, this value is reloaded into the timer counter after the timer counter reaches 0. It may be updated at any time; the new value will be written to the counter immediately. Writing a load value of 0 will disable the timer, except in free-running mode. |  |
|--|--|--|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|

**TMR1VAL: Timer 1 Counter Value (offset: 0x0024)**

| Bits  | Type | Name   | Description                                                                                                                       | Initial value |
|-------|------|--------|-----------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:16 | -    | -      | Reserved                                                                                                                          | -             |
| 15:0  | RO   | TMRVAL | Timer Counter Value<br>This register contains the current value of the timer. During functional operation, writes have no effect. | 0xffff        |

**TMR1CTL: Timer 1 Control (offset: 0x0028)**

| Bits  | Type                  | Name           | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | Initial value |                       |   |              |   |                  |   |                  |   |                   |   |   |   |   |    |                      |    |                      |     |
|-------|-----------------------|----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|-----------------------|---|--------------|---|------------------|---|------------------|---|-------------------|---|---|---|---|----|----------------------|----|----------------------|-----|
| 31:16 | -                     | -              | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | -             |                       |   |              |   |                  |   |                  |   |                   |   |   |   |   |    |                      |    |                      |     |
| 15    | RW                    | TESTEN         | Reserved for Test<br>This bit should be written with a zero                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | 0x0           |                       |   |              |   |                  |   |                  |   |                   |   |   |   |   |    |                      |    |                      |     |
| 14:8  | -                     | -              | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | -             |                       |   |              |   |                  |   |                  |   |                   |   |   |   |   |    |                      |    |                      |     |
| 7     | RW                    | ENABLE         | Timer Enable<br>0: Disable the timer. The timer will stop counting and will retain its current value.<br>1: Enable the timer. The timer will begin counting from its current value.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | 0x0           |                       |   |              |   |                  |   |                  |   |                   |   |   |   |   |    |                      |    |                      |     |
| 6     | RW                    | WD_TIMEOUT_SRC | Watchdog timeout alarm source<br>0: From Timer 1<br>1: From PMU watch dog timer                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | 0x0           |                       |   |              |   |                  |   |                  |   |                   |   |   |   |   |    |                      |    |                      |     |
| 5:4   | RW                    | MODE           | Timer Mode<br>0: Free-running<br>1: Periodic<br>2: Time-out<br>3: Watchdog                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | 0x0           |                       |   |              |   |                  |   |                  |   |                   |   |   |   |   |    |                      |    |                      |     |
| 3     | -                     | -              | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | -             |                       |   |              |   |                  |   |                  |   |                   |   |   |   |   |    |                      |    |                      |     |
| 2:0   | RW                    | PRESCALE       | <div>Timer Clock Pre-scale<br/>These bits are used to scale the timer clock in order to achieve higher resolution or longer timer periods. Their definitions are below.</div> <table><thead><tr><th>Value</th><th>Timer Clock Frequency</th></tr></thead><tbody><tr><td>0</td><td>System clock</td></tr><tr><td>1</td><td>System clock / 4</td></tr><tr><td>2</td><td>System clock / 8</td></tr><tr><td>3</td><td>System clock / 16</td></tr><tr><td>.</td><td>.</td></tr><tr><td>.</td><td>.</td></tr><tr><td>14</td><td>System clock / 32768</td></tr><tr><td>15</td><td>System clock / 65536</td></tr></tbody></table> <div>Note: The pre-scale value should not be changed unless the timer is disabled.</div> | Value         | Timer Clock Frequency | 0 | System clock | 1 | System clock / 4 | 2 | System clock / 8 | 3 | System clock / 16 | . | . | . | . | 14 | System clock / 32768 | 15 | System clock / 65536 | 0x0 |
| Value | Timer Clock Frequency |                |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |               |                       |   |              |   |                  |   |                  |   |                   |   |   |   |   |    |                      |    |                      |     |
| 0     | System clock          |                |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |               |                       |   |              |   |                  |   |                  |   |                   |   |   |   |   |    |                      |    |                      |     |
| 1     | System clock / 4      |                |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |               |                       |   |              |   |                  |   |                  |   |                   |   |   |   |   |    |                      |    |                      |     |
| 2     | System clock / 8      |                |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |               |                       |   |              |   |                  |   |                  |   |                   |   |   |   |   |    |                      |    |                      |     |
| 3     | System clock / 16     |                |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |               |                       |   |              |   |                  |   |                  |   |                   |   |   |   |   |    |                      |    |                      |     |
| .     | .                     |                |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |               |                       |   |              |   |                  |   |                  |   |                   |   |   |   |   |    |                      |    |                      |     |
| .     | .                     |                |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |               |                       |   |              |   |                  |   |                  |   |                   |   |   |   |   |    |                      |    |                      |     |
| 14    | System clock / 32768  |                |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |               |                       |   |              |   |                  |   |                  |   |                   |   |   |   |   |    |                      |    |                      |     |
| 15    | System clock / 65536  |                |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |               |                       |   |              |   |                  |   |                  |   |                   |   |   |   |   |    |                      |    |                      |     |

### 3.6 Interrupt Controller

#### 3.6.1 Features

- Support a central point for interrupt aggregation for platform related blocks
- Separated interrupt enable and disable registers
- Support global disable function
- 2-level Interrupt priority selection
- Each interrupt source can be directed to IRQ#0 or IRQ#1

Note : RT5350 supports MIPS 24K's vector interrupt mechanism.

There are 6 hardware interrupts supported by MIPS 24K. The interrupt allocation is shown below:

| MIPS H/W interrupt pins | Connect to                             | Remark           |
|-------------------------|----------------------------------------|------------------|
| HW_INT#5                | Timer interrupt                        | Highest priority |
| HW_INT#4                | 802.11n NIC                            |                  |
| HW_INT#3                | FE                                     |                  |
| HW_INT#2                | Reserved                               |                  |
| HW_INT#1                | Other high priority interrupts (IRQ#1) |                  |
| HW_INT#0                | Other low priority interrupts (IRQ#0)  | Lowest priority  |

#### 3.6.2 Block Diagram

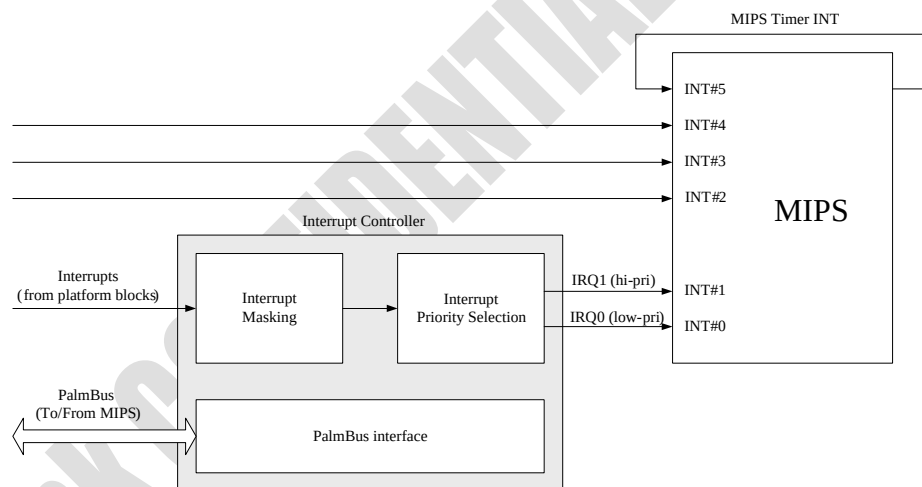


Fig. 3-6-1 Interrupt Controller Block Diagram

#### 3.6.3 Register Description (base: 0x1000\_0200)

IRQ0STAT: Interrupt Type 0 Status after Enable Mask (offset: 0x0000)

| Bits  | Type | Name | Description                                 | Initial value |
|-------|------|------|---------------------------------------------|---------------|
| 31:20 | -    | -    | Reserved                                    | -             |
| 19    | RO   | UDEV | USB device interrupt status after mask      | 0x0           |
| 18    | RO   | UHST | USB host interrupt status after mask        | 0x0           |
| 17    | RO   | ESW  | Ethernet Swtich interrupt status after mask | 0x0           |
| 16    | -    | -    | Reserved                                    | -             |
| 15:13 | -    | -    | Reserved                                    | -             |

|    |    |          |                                                      |     |
|----|----|----------|------------------------------------------------------|-----|
| 12 | RO | UARTLITE | UARTLITE interrupt status after mask                 | 0x0 |
| 11 | RO | -        | Reserved                                             | -   |
| 10 | RO | I2S      | I2S interrupt status after mask                      | 0x0 |
| 9  | RO | PC       | MIPS performance counter interrupt status after mask | 0x0 |
| 8  | RO | -        | Reserved                                             | -   |
| 7  | RO | DMA      | DMA interrupt status after mask                      | 0x0 |
| 6  | RO | PIO      | PIO interrupt status after mask                      | 0x0 |
| 5  | RO | UART     | UART interrupt status after mask                     | 0x0 |
| 4  | RO | PCM      | PCM interrupt status after mask                      | 0x0 |
| 3  | RO | ILL_ACC  | Illegal access interrupt status after mask           | 0x0 |
| 2  | RO | WDTIMER  | Watch dog timer interrupt status after mask          | 0x0 |
| 1  | RO | TIMER0   | Timer 0 interrupt status after mask                  | 0x0 |
| 0  | RO | SYSCTL   | System control interrupt status after mask           | 0x0 |

These bits are set if the corresponding interrupt is asserted from the source and with following two conditions

- The interrupt is not masked (bit not set in the INTDIS register)
- The interrupt type is set to INTO (in the INTTYPE register).

Note that write to these bits are ignored and each bit cannot be simultaneously active in both the IRQ0STAT and IRQ1STAT registers.

IRQ1STAT: Interrupt Type 1 Status after Enable Mask (offset: 0x0004)

| Bits  | Type | Name     | Description                                          | Initial value |
|-------|------|----------|------------------------------------------------------|---------------|
| 31:20 | -    | -        | Reserved                                             | -             |
| 19    | RO   | UDEV     | USB device interrupt status after mask               | 0x0           |
| 18    | RO   | UHST     | USB host interrupt status after mask                 | 0x0           |
| 17    | RO   | ESW      | Ethernet Swtich interrupt status after mask          | 0x0           |
| 16    | -    | -        | Reserved                                             | -             |
| 15:13 | -    | -        | Reserved                                             | -             |
| 12    | RO   | UARTLITE | UARTLITE interrupt status after mask                 | 0x0           |
| 11    | -    | -        | Reserved                                             | -             |
| 10    | RO   | I2S      | I2S interrupt status after mask                      | 0x0           |
| 9     | RO   | PC       | MIPS performance counter interrupt status after mask | 0x0           |
| 8     | -    | -        | Reserved                                             | -             |
| 7     | RO   | DMA      | DMA interrupt status after mask                      | 0x0           |
| 6     | RO   | PIO      | PIO interrupt status after mask                      | 0x0           |
| 5     | RO   | UART     | UART interrupt status after mask                     | 0x0           |
| 4     | RO   | PCM      | PCM interrupt status after mask                      | 0x0           |
| 3     | RO   | ILL_ACC  | Illegal access interrupt status after mask           | 0x0           |
| 2     | RO   | WDTIMER  | Watch dog timer interrupt status after mask          | 0x0           |
| 1     | RO   | TIMER0   | Timer 0 interrupt status after mask                  | 0x0           |
| 0     | RO   | SYSCTL   | System control interrupt status after mask           | 0x0           |

These bits are set if the corresponding interrupt is asserted from the source and with following two conditions

- The interrupt is not masked (bit not set in the INTDIS register)
- The interrupt type is set to INT1 (in the INTTYPE register).

Note that writing to these bits is ignored and each bit cannot be simultaneously active in both the IRQ0STAT and IRQ1STAT registers.

INTTYPE: Interrupt Type (offset: 0x0020)

| Bits  | Type | Name | Description                           | Initial value |
|-------|------|------|---------------------------------------|---------------|
| 31:20 | -    | -    | Reserved                              | -             |
| 19    | RW   | UDEV | USB device interrupt status type      | 0x0           |
| 18    | RW   | UHST | USB host interrupt status type        | 0x0           |
| 17    | RW   | ESW  | Ethernet Swtich interrupt status type | 0x0           |
| 16    | -    | -    | Reserved                              | -             |

|       |    |          |                                                |     |
|-------|----|----------|------------------------------------------------|-----|
| 15:13 | -  | -        | Reserved                                       | -   |
| 12    | RW | UARTLITE | UARTLITE interrupt status type                 | 0x0 |
| 11    | -  | -        | Reserved                                       | -   |
| 10    | RW | I2S      | I2S interrupt status type                      | 0x0 |
| 9     | RW | PC       | MIPS performance counter interrupt status type | 0x0 |
| 8     | -  | -        | Reserved                                       | -   |
| 7     | RW | DMA      | DMA interrupt status after type                | 0x0 |
| 6     | RW | PIO      | PIO interrupt status after type                | 0x0 |
| 5     | RW | UART     | UART interrupt status type                     | 0x0 |
| 4     | RW | PCM      | PCM interrupt status type                      | 0x0 |
| 3     | RW | ILL_ACC  | Illegal access interrupt status type           | 0x0 |
| 2     | RW | WDTIMER  | Watch dog timer interrupt status type          | 0x0 |
| 1     | RW | TIMER0   | Timer 0 interrupt status type                  | 0x0 |
| 0     | RW | SYSCCTL  | System control interrupt status type           | 0x0 |

These bits control whether an interrupt is IRQ0 or IRQ1. The interrupt type may be changed at any time; if the interrupt type is changed while the interrupt is active, the interrupt is immediately redirected.

INTRAW: Raw Interrupt Status before Enable Mask (offset: 0x0030)

| Bits  | Type | Name     | Description                                           | Initial value |
|-------|------|----------|-------------------------------------------------------|---------------|
| 31:20 | -    | -        | Reserved                                              | -             |
| 19    | RO   | UDEV     | USB device interrupt status before mask               | 0x0           |
| 18    | RO   | UHST     | USB host interrupt status before mask                 | 0x0           |
| 17    | RO   | ESW      | Ethernet Swtich interrupt status before mask          | 0x0           |
| 16    | -    | -        | Reserved                                              | -             |
| 15:13 | -    | -        | Reserved                                              | -             |
| 12    | RO   | UARTLITE | UARTLITE interrupt status before mask                 | 0x0           |
| 11    | RO   | -        | Reserved                                              | -             |
| 10    | RO   | I2S      | I2S interrupt status before r mask                    | 0x0           |
| 9     | RO   | PC       | MIPS performance counter interrupt status before mask | 0x0           |
| 8     | -    | -        | Reserved                                              | -             |
| 7     | RO   | DMA      | DMA interrupt status before mask                      | 0x0           |
| 6     | RO   | PIO      | PIO interrupt status before mask                      | 0x0           |
| 5     | RO   | UART     | UART interrupt status before mask                     | -             |
| 4     | RO   | PCM      | PCM interrupt status before mask                      | 0x0           |
| 3     | RO   | ILL_ACC  | Illegal access interrupt status before mask           | 0x0           |
| 2     | RO   | WDTIMER  | Watch dog timer interrupt status before mask          | 0x0           |
| 1     | RO   | TIMER0   | Timer 0 interrupt status before mask                  | 0x0           |
| 0     | RO   | SYSCCTL  | System control interrupt status before mask           | 0x0           |

These bits are set if the corresponding interrupt is asserted from the source. The status bit is set if the interrupt is active, even if it is masked, and regardless of the interrupt type. This provides a single-access snapshot of all active interrupts for implementation of a polling system.

INTENA: Interrupt Enable (offset: 0x0034)

| Bits  | Type | Name   | Description                                                                                                                                                                                        | Initial value |
|-------|------|--------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31    | RW   | GLOBAL | Global interrupt enable<br>Writing a '1' to this bit allows interrupt masking to be performed based on each interrupt's individual enable mask. A read returns the global status ('1' if enabled). | 0x0           |
| 30:20 | -    | -      | Reserved                                                                                                                                                                                           | -             |
| 19    | RW   | UDEV   | USB device interrupt enable                                                                                                                                                                        | 0x0           |
| 18    | RW   | UHST   | USB host interrupt enable                                                                                                                                                                          | 0x0           |
| 17    | RW   | ESW    | Ethernet Swtich interrupt enable                                                                                                                                                                   | 0x0           |
| 16    | -    | -      | Reserved                                                                                                                                                                                           | -             |
| 15:13 | -    | -      | Reserved                                                                                                                                                                                           | -             |

|    |    |          |                                           |     |
|----|----|----------|-------------------------------------------|-----|
| 12 | RW | UARTLITE | UARTLITE interrupt enable                 | 0x0 |
| 11 | -  | -        | Reserved                                  | -   |
| 10 | RW | I2S      | I2S interrupt enable                      | 0x0 |
| 9  | RW | PC       | MIPS performance counter interrupt enable | 0x0 |
| 8  | -  | -        | Reserved                                  | -   |
| 7  | RW | DMA      | DMA interrupt enable                      | 0x0 |
| 6  | RW | PIO      | PIO interrupt enable                      | 0x0 |
| 5  | RW | UART     | UART interrupt enable                     | 0x0 |
| 4  | RW | PCM      | PCM interrupt enable                      | 0x0 |
| 3  | RW | ILL_ACC  | Illegal access interrupt enable           | 0x0 |
| 2  | RW | WDTIMER  | Watch dog timer interrupt enable          | 0x0 |
| 1  | RW | TIMER0   | Timer 0 interrupt enable                  | 0x0 |
| 0  | RW | SYSCTL   | System control interrupt enable           | 0x0 |

Writing a '1' to these bits (except the GLOBAL bit) will enable the mask for the corresponding interrupt. The interrupt is asserted and the bit is set in the IRQ0STAT or IRQ1STAT registers if an interrupt is enabled. Writes of '0' are ignored. Reading either the INTENA or INTDIS register will return the current mask, where an interrupt is masked (disabled) if the bit is 'zero', and unmasked (enabled) if the bit is 'one'.

INTDIS: Interrupt Disable (offset: 0x0038)

| Bits  | Type | Name     | Description                                                                                                                                                                                           | Initial value |
|-------|------|----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31    | RW   | GLOBAL   | Global interrupt disable<br>Writing a '1' to this bit allows interrupt masking to be performed based on each interrupt's individual Disable mask. A read returns the global status ('1' if Disabled). | 0x0           |
| 30:20 | -    | -        | Reserved                                                                                                                                                                                              | -             |
| 19    | RW   | UDEV     | USB device interrupt status disable                                                                                                                                                                   | 0x0           |
| 18    | RW   | UHST     | USB host interrupt status disable                                                                                                                                                                     | 0x0           |
| 17    | RW   | ESW      | Ethernet Switch interrupt disable                                                                                                                                                                     | 0x0           |
| 16    | -    | -        | Reserved                                                                                                                                                                                              | -             |
| 15:13 | -    | -        | Reserved                                                                                                                                                                                              | -             |
| 12    | RW   | UARTLITE | UARTLITE interrupt s disable                                                                                                                                                                          | 0x0           |
| 11    | -    | -        | Reserved                                                                                                                                                                                              | -             |
| 10    | RW   | I2S      | I2S interrupt disable                                                                                                                                                                                 | 0x0           |
| 9     | RW   | PC       | MIPS performance counter interrupt disable                                                                                                                                                            | 0x0           |
| 8     | RW   | NAND     | NAND flash controller interrupt disable                                                                                                                                                               | 0x0           |
| 7     | RW   | DMA      | DMA interrupt disable                                                                                                                                                                                 | 0x0           |
| 6     | RW   | PIO      | PIO interrupt disable                                                                                                                                                                                 | 0x0           |
| 5     | RW   | UART     | UART interrupt disable                                                                                                                                                                                | 0x0           |
| 4     | RW   | PCM      | PCM interrupt disable                                                                                                                                                                                 | 0x0           |
| 3     | RW   | ILL_ACC  | Illegal access interrupt disable                                                                                                                                                                      | 0x0           |
| 2     | RW   | WDTIMER  | Watch dog timer interrupt disable                                                                                                                                                                     | 0x0           |
| 1     | RW   | TIMER0   | Timer 0 interrupt disable                                                                                                                                                                             | 0x0           |
| 0     | RW   | SYSCTL   | System control interrupt disable                                                                                                                                                                      | 0x0           |

Writing a '1' to these bits (except the GLOBAL bit) will disable the mask for the corresponding interrupt. The interrupt is asserted and the bit is set in the IRQ0STAT or IRQ1STAT registers if an interrupt is enabled. Writing '0' is ignored. Reading either the INTENA or INTDIS register will return the current mask, where an interrupt is masked (disabled) if the bit is 'zero', and unmasked (enabled) if the bit is 'one'.

### 3.7 System Tick Counter

#### 3.7.1 Register Description (base: 0x1000\_0d00)

STCK\_CNT\_CFG : MIPS Configuration Register (offset: 0x0000)

| Bits | Type | Name       | Description                                                                                                                       | Initial value |
|------|------|------------|-----------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:2 | -    | -          | Reserved                                                                                                                          | 0x0           |
| 1    | RW   | EXT_STK_EN | External system tick enable<br>0: Use MIPS internal timer interrupt<br>1: Use external timer interrupt from external MIPS counter | 0x0           |
| 0    | RW   | CNT_EN     | Counter enable<br>0: Disable free run counter<br>1: Enable free run counter                                                       | 0x0           |

CMP\_CNT : MIPS Compare Register (offset: 0x0004)

| Bits  | Type | Name    | Description                                                                                                                                          | Initial value |
|-------|------|---------|------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:16 | -    | -       | Reserved                                                                                                                                             | 0x0           |
| 15:0  | RW   | CMP_CNT | If the <i>Counter</i> ever equals Compare, then the timer circuit generates an interrupt. The interrupt remain active until Compare is written again | 0x0           |

CNT : MIPS Counter Register (offset: 0x0008)

| Bits  | Type | Name | Description                                                                                                                               | Initial value |
|-------|------|------|-------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:16 | -    | -    | Reserved                                                                                                                                  | 0x0           |
| 15:0  | RW   | CNT  | This counter increase by 1 every 20us(50KHz). Count is writable/readable and will carry on counting from whatever value is loaded into it | 0x0           |

### 3.8 UART

#### 3.8.1 Features

- 16550-compatible register set, except for Divisor Latch register
- 5-8 data bits
- 1-2 stop bits (1 or 2 stop bits are supported with 5 data bits)
- Even, odd, stick or no parity
- All standard baud rates up to 345600 b/s
- 16-byte receive buffer
- 16-byte transmit buffer
- Receive buffer threshold interrupt
- Transmit buffer threshold interrupt
- False start bit detection in asynchronous mode
- Internal diagnostic capabilities
- Break simulation
- Loop-back control for communications link fault isolation

### 3.8.2 Block Diagram

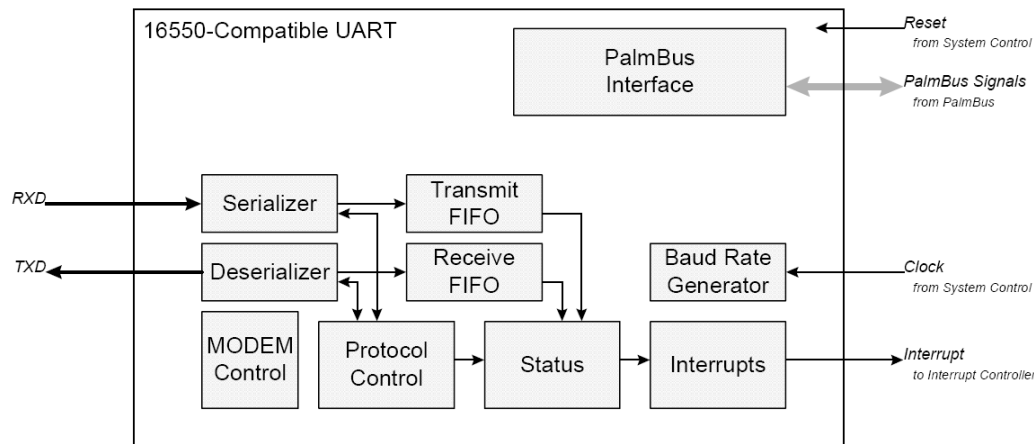


Fig. 5-8-1 UART block diagram

### 3.8.3 Register Description (base: 0x1000\_0500)

RBR : Receive Buffer Register (offset: 0x0000)

| Bits | Type | Name     | Description                                                                                                                                                                                                                                                                                                        | Initial value |
|------|------|----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:8 | -    | -        | Reserved                                                                                                                                                                                                                                                                                                           | 0x0           |
| 7    | RO   | RXD[7:0] | Receive Buffer Data<br>Receive data. Data is transferred to this register from the receive shift register after a full character is received. The OE bit in the LSR register is set, indication a receive buffer overrun, if the contents of this register has not been read before another character is received. | 0x0           |

TBR : Transmit Buffer Register (offset: 0x0004)

| Bits | Type | Name     | Description                                                                                                                                                                                                                                             | Initial value |
|------|------|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:8 | -    | -        | Reserved                                                                                                                                                                                                                                                | 0x0           |
| 7    | WO   | TXD[7:0] | Transmit Buffer Data<br>Transmit data. When a character is written to this register, it is stored in the transmitter holding register; if the transmitter register is empty, the character is moved to the transmitter register, starting transmission. | 0x0           |

IER : Interrupt Enable Register (offset: 0x0008)

| Bits | Type | Name  | Description                                                                                                                                                                           | Initial value |
|------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:4 | -    | -     | Reserved                                                                                                                                                                              | 0x0           |
| 3    | RW   | EDSSI | Enable Modem Interrupt<br>1: modem status (DCD, RI, DSR, CTS, DDCD, TERI, DDSR, and DCTS) intrupts.<br>0: Disable modem status (DCD, RI, DSR, CTS, DDCD, TDDSR, and DCTS) interrupts. | 0x0           |
| 2    | RW   | ELSI  | Enable Receiver Line Status Interrupt<br>1: Enable line status (OE, PE, FE, and BI) interrupts.<br>0: Disable line status (OE, PE, FE, and BI) interrupts.                            | 0x0           |
| 1    | RW   | ETBEI | Enable Transmitter Buffer Line Status Interrupt<br>1: Enable transmit buffer empty (THRE) interrupt.<br>0: Disable transmit buffer empty (THRE) interrupt.                            | 0x0           |



|   |    |       |                                                                                                                                                                     |     |
|---|----|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|
| 0 | RW | ERBFI | Enable Receiver Buffer Empty Interrupt<br>1: Enable data ready (DR) or character time-out interrupt.<br>0: Disable data ready (DR) or character time-out interrupt. | 0x0 |
|---|----|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|

**IIR : Interrupt Identification Register (offset: 0x000c)**

| Bits | Type     | Name                  | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | Initial value |          |      |        |   |  |           |  |   |  |           |  |   |  |           |  |   |  |           |  |   |   |                      |             |   |   |                      |    |   |   |                       |      |   |  |           |  |     |
|------|----------|-----------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|----------|------|--------|---|--|-----------|--|---|--|-----------|--|---|--|-----------|--|---|--|-----------|--|---|---|----------------------|-------------|---|---|----------------------|----|---|---|-----------------------|------|---|--|-----------|--|-----|
| 31:8 | -        | -                     | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | 0x0           |          |      |        |   |  |           |  |   |  |           |  |   |  |           |  |   |  |           |  |   |   |                      |             |   |   |                      |    |   |   |                       |      |   |  |           |  |     |
| 7:6  | RO       | FIFOENA[1:0]          | FIFOs Enabled<br>FIFOs Enabled. These bits reflect the FIFO enable bit setting in the FIFO Control Register. When the FIFO enable bit is set, both of these bits will be set high to a value of '11'. When the FIFO enable bit is cleared, both of these bits will be set low to a value of '00'.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | 0x0           |          |      |        |   |  |           |  |   |  |           |  |   |  |           |  |   |  |           |  |   |   |                      |             |   |   |                      |    |   |   |                       |      |   |  |           |  |     |
| 5:4  | -        | -                     | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | 0x0           |          |      |        |   |  |           |  |   |  |           |  |   |  |           |  |   |  |           |  |   |   |                      |             |   |   |                      |    |   |   |                       |      |   |  |           |  |     |
| 3:1  | RO       | INTID[2:0]            | <div>Interrupt Identifier<br/>Interrupt ID. These bits provide a snapshot of the interrupt type, and may be used as the offset into an interrupt vector table. The interrupt encoding is given below.</div> <table><tr><th>ID</th><th>Priority</th><th>Type</th><th>Source</th></tr><tr><td>7</td><td></td><td>Undefined</td><td></td></tr><tr><td>6</td><td></td><td>Undefined</td><td></td></tr><tr><td>5</td><td></td><td>Undefined</td><td></td></tr><tr><td>4</td><td></td><td>Undefined</td><td></td></tr><tr><td>3</td><td>1</td><td>Receiver Line Status</td><td>OE,PE,FE,BI</td></tr><tr><td>2</td><td>2</td><td>Receiver Buffer Full</td><td>DR</td></tr><tr><td>1</td><td>3</td><td>Transmit buffer Empty</td><td>THRE</td></tr><tr><td>0</td><td></td><td>Undefined</td><td></td></tr></table> <div>If more than one category of interrupt is asserted, only the highest priority ID will be given. The line and Modem status interrupts are cleared by reading the corresponding status register (LSR, MSR). The Receive Buffer Full interrupt will be cleared when all of the data is read from the receiver buffer. The Transmitter Buffer empty will be cleared when data is written to the TBR register. See also "Interrupt Priorities".</div> | ID            | Priority | Type | Source | 7 |  | Undefined |  | 6 |  | Undefined |  | 5 |  | Undefined |  | 4 |  | Undefined |  | 3 | 1 | Receiver Line Status | OE,PE,FE,BI | 2 | 2 | Receiver Buffer Full | DR | 1 | 3 | Transmit buffer Empty | THRE | 0 |  | Undefined |  | 0x0 |
| ID   | Priority | Type                  | Source                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |               |          |      |        |   |  |           |  |   |  |           |  |   |  |           |  |   |  |           |  |   |   |                      |             |   |   |                      |    |   |   |                       |      |   |  |           |  |     |
| 7    |          | Undefined             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |               |          |      |        |   |  |           |  |   |  |           |  |   |  |           |  |   |  |           |  |   |   |                      |             |   |   |                      |    |   |   |                       |      |   |  |           |  |     |
| 6    |          | Undefined             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |               |          |      |        |   |  |           |  |   |  |           |  |   |  |           |  |   |  |           |  |   |   |                      |             |   |   |                      |    |   |   |                       |      |   |  |           |  |     |
| 5    |          | Undefined             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |               |          |      |        |   |  |           |  |   |  |           |  |   |  |           |  |   |  |           |  |   |   |                      |             |   |   |                      |    |   |   |                       |      |   |  |           |  |     |
| 4    |          | Undefined             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |               |          |      |        |   |  |           |  |   |  |           |  |   |  |           |  |   |  |           |  |   |   |                      |             |   |   |                      |    |   |   |                       |      |   |  |           |  |     |
| 3    | 1        | Receiver Line Status  | OE,PE,FE,BI                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |               |          |      |        |   |  |           |  |   |  |           |  |   |  |           |  |   |  |           |  |   |   |                      |             |   |   |                      |    |   |   |                       |      |   |  |           |  |     |
| 2    | 2        | Receiver Buffer Full  | DR                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |               |          |      |        |   |  |           |  |   |  |           |  |   |  |           |  |   |  |           |  |   |   |                      |             |   |   |                      |    |   |   |                       |      |   |  |           |  |     |
| 1    | 3        | Transmit buffer Empty | THRE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |               |          |      |        |   |  |           |  |   |  |           |  |   |  |           |  |   |  |           |  |   |   |                      |             |   |   |                      |    |   |   |                       |      |   |  |           |  |     |
| 0    |          | Undefined             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |               |          |      |        |   |  |           |  |   |  |           |  |   |  |           |  |   |  |           |  |   |   |                      |             |   |   |                      |    |   |   |                       |      |   |  |           |  |     |
| 0    | RO       | INTPEND               | Interrupt Pending<br>0: An interrupt bit is set and is not masked.<br>1: No interrupts are pending.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | 0x1           |          |      |        |   |  |           |  |   |  |           |  |   |  |           |  |   |  |           |  |   |   |                      |             |   |   |                      |    |   |   |                       |      |   |  |           |  |     |

**FCR : FIFO Control Register (offset: 0x0010)**

| Bits | Type | Name | Description | Initial value |
|------|------|------|-------------|---------------|
| 31:8 | -    | -    | Reserved    | 0x0           |

| 7:6    | RW            | RXTRIG[1:0] | <p>Receiver Trigger Level</p> <p>The data ready interrupt (DR) will be asserted when the receive buffer depth is equal to the number of characters programmed in the trigger register. The trigger level encoding is as follows:</p> <table><tr><th>RXTRIG</th><th>Trigger Level</th></tr><tr><td>0</td><td>1</td></tr><tr><td>1</td><td>4</td></tr><tr><td>2</td><td>8</td></tr><tr><td>3</td><td>14</td></tr></table> <p>Note: This register is not used if the receive FIFO is disabled.</p> | RXTRIG | Trigger Level | 0 | 1 | 1 | 4 | 2 | 8 | 3 | 14 | 0x0 |
|--------|---------------|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|---------------|---|---|---|---|---|---|---|----|-----|
| RXTRIG | Trigger Level |             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |        |               |   |   |   |   |   |   |   |    |     |
| 0      | 1             |             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |        |               |   |   |   |   |   |   |   |    |     |
| 1      | 4             |             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |        |               |   |   |   |   |   |   |   |    |     |
| 2      | 8             |             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |        |               |   |   |   |   |   |   |   |    |     |
| 3      | 14            |             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |        |               |   |   |   |   |   |   |   |    |     |
| 5:4    | RW            | TXTRIG[1:0] | <p>Transmitter Trigger Level</p> <p>The THRE interrupt will be asserted if the transmitter buffer depth is less than or equal to the number of characters programmed in the trigger register. The trigger level encoding is as follows:</p> <table><tr><th>TXTRIG</th><th>Trigger Level</th></tr><tr><td>0</td><td>1</td></tr><tr><td>1</td><td>4</td></tr><tr><td>2</td><td>8</td></tr><tr><td>3</td><td>12</td></tr></table>                                                                  | TXTRIG | Trigger Level | 0 | 1 | 1 | 4 | 2 | 8 | 3 | 12 | 0x0 |
| TXTRIG | Trigger Level |             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |        |               |   |   |   |   |   |   |   |    |     |
| 0      | 1             |             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |        |               |   |   |   |   |   |   |   |    |     |
| 1      | 4             |             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |        |               |   |   |   |   |   |   |   |    |     |
| 2      | 8             |             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |        |               |   |   |   |   |   |   |   |    |     |
| 3      | 12            |             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |        |               |   |   |   |   |   |   |   |    |     |
| 3      | RW            | DMAMODE     | <p>Enable DMA transfers</p> <p>This bit is writeable and readable, but has no other hardware function.</p>                                                                                                                                                                                                                                                                                                                                                                                      | 0x0    |               |   |   |   |   |   |   |   |    |     |
| 2      | RW            | TXRST       | <p>Transmitter Reset</p> <p>Writing a '1' to this bit will clear the transmit FIFO and reset the transmitter status. The shift register is not cleared.</p>                                                                                                                                                                                                                                                                                                                                     | 0x0    |               |   |   |   |   |   |   |   |    |     |
| 1      | RW            | RXRST       | <p>Receive Reset</p> <p>Writing a '1' to this bit will clear the receive FIFO and reset the receiver status. The shift register is not cleared.</p>                                                                                                                                                                                                                                                                                                                                             | 0x0    |               |   |   |   |   |   |   |   |    |     |
| 0      | RW            | FIFOENA     | <p>0: The Transmit and Receive FIFOs have the effective depth of one character.</p> <p>1: The Transmit and Receive FIFOs are enabled.</p> <p>Note: The FIFO status and data are automatically cleared when this bit is changed.</p>                                                                                                                                                                                                                                                             | 0x0    |               |   |   |   |   |   |   |   |    |     |

LCR : Line Control Register (offset: 0x0014)

| Bits | Type | Name   | Description                                                                                                               | Initial value |
|------|------|--------|---------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:8 | -    | -      | Reserved                                                                                                                  | 0x0           |
| 7    | RW   | DLAB   | <p>Divisor Latch Access Bit</p> <p>This bit has no functionality, and is retained for compatibility only</p>              | 0x0           |
| 6    | RW   | SETBRK | <p>Set Break Condition</p> <p>0: Normal functionality.</p> <p>1: Force TXD pin to '0'. Transmitter otherwise operates</p> | 0x0           |

|     |    |          |                                                                                                                                                                                                                         |     |
|-----|----|----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|
|     |    |          | normally.                                                                                                                                                                                                               |     |
| 5   | RW | FORCEPAR | Force Parity Bit<br>0: Normal functionality.<br>1: If even parity is selected, the (transmitted and checked) parity is forced to '0'; if odd parity is selected, the (transmitted and checked) parity is forced to '1'. | 0x0 |
| 4   | RW | EPS      | Even Parity Select<br>0: Odd parity selected (checksum, including parity is '1').<br>1: Even parity selected (checksum, including parity is '0').<br>Note: This bit is ignored if the PEN bit is '0'.                   | 0x0 |
| 3   | RW | PEN      | Parity Enable<br>0: Parity is not transmitted or checked.<br>1: Parity is generated (transmit), and checked (receive).                                                                                                  | 0x0 |
| 2   | RW | STB      | Stop Bit Select<br>0: 1 stop bit is transmitted and received.<br>1: 1.5 stop bits are transmitted and received if WLS is '0'; 2 stop bits are transmitted and received if WLS is '1', '2', or '3'.                      | 0x0 |
| 1:0 | RW | WLS[1:0] | Word Length Select<br>0: Each character is 5 bits in length<br>1: Each character is 6 bits in length<br>2: Each character is 7 bits in length<br>3: Each character is 8 bits in length                                  | 0x0 |

MCR : Modem Control Register (offset: 0x0018)

| Bits   | Type                    | Name | Description                                                                                                                                                                                                                                                                                                                                                                                                                                            | Initial value |                         |     |     |      |      |      |      |       |     |       |      |     |
|--------|-------------------------|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|-------------------------|-----|-----|------|------|------|------|-------|-----|-------|------|-----|
| 31:5   | -                       | -    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                               | 0x0           |                         |     |     |      |      |      |      |       |     |       |      |     |
| 4      | RW                      | LOOP | <div>Loop-back Mode Enable<br/>0: Normal Operation.<br/>1: The UART is put into loop-back mode, used for self-test: TXD pin is driven high; the TXD signal connections are made internally</div> <table><tr><td>Signal</td><td>Wrapped back through...</td></tr><tr><td>TXD</td><td>RXD</td></tr><tr><td>DTRN</td><td>DSRN</td></tr><tr><td>RTSN</td><td>CTSN</td></tr><tr><td>OUT1N</td><td>RIN</td></tr><tr><td>OUT2N</td><td>DCDN</td></tr></table> | Signal        | Wrapped back through... | TXD | RXD | DTRN | DSRN | RTSN | CTSN | OUT1N | RIN | OUT2N | DCDN | 0x0 |
| Signal | Wrapped back through... |      |                                                                                                                                                                                                                                                                                                                                                                                                                                                        |               |                         |     |     |      |      |      |      |       |     |       |      |     |
| TXD    | RXD                     |      |                                                                                                                                                                                                                                                                                                                                                                                                                                                        |               |                         |     |     |      |      |      |      |       |     |       |      |     |
| DTRN   | DSRN                    |      |                                                                                                                                                                                                                                                                                                                                                                                                                                                        |               |                         |     |     |      |      |      |      |       |     |       |      |     |
| RTSN   | CTSN                    |      |                                                                                                                                                                                                                                                                                                                                                                                                                                                        |               |                         |     |     |      |      |      |      |       |     |       |      |     |
| OUT1N  | RIN                     |      |                                                                                                                                                                                                                                                                                                                                                                                                                                                        |               |                         |     |     |      |      |      |      |       |     |       |      |     |
| OUT2N  | DCDN                    |      |                                                                                                                                                                                                                                                                                                                                                                                                                                                        |               |                         |     |     |      |      |      |      |       |     |       |      |     |
| 3      | RW                      | OUT2 | <div>Out2 Value<br/>0: OUT2N pin is driven to a high level.<br/>1: OUT2N pin is driven to a low level.<br/>Note: This bit is only functional in loop-back mode.</div>                                                                                                                                                                                                                                                                                  | 0x0           |                         |     |     |      |      |      |      |       |     |       |      |     |
| 2      | RW                      | OUT1 | <div>Out1 Value<br/>0: OUT1N pin is driven to a high level.<br/>1: OUT1N pin is driven to a low level.<br/>Note: This bit is only functional in loop-back mode.</div>                                                                                                                                                                                                                                                                                  | 0x0           |                         |     |     |      |      |      |      |       |     |       |      |     |
| 1      | RW                      | RTS  | <div>Out1 Value<br/>0: RTSN pin is driven to a high level.<br/>1: RTSN pin is driven to a low level.</div>                                                                                                                                                                                                                                                                                                                                             | 0x0           |                         |     |     |      |      |      |      |       |     |       |      |     |
| 1      | RW                      | DTR  | <div>Reserved<br/>0: DTRN pin is driven to a high level.<br/>1: DTRN pin is driven to a low level.</div>                                                                                                                                                                                                                                                                                                                                               | 0x0           |                         |     |     |      |      |      |      |       |     |       |      |     |

LSR : Line Status Register (offset: 0x001c)

| Bits | Type | Name | Description | Initial value |
|------|------|------|-------------|---------------|
|------|------|------|-------------|---------------|

|      |    |          |                                                                                                                                                                                                                                         |     |
|------|----|----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|
| 31:8 | -  | -        | Reserved                                                                                                                                                                                                                                | 0x0 |
| 7    | RC | ERINFIFO | The FIFO contains data which had a parity or framing error<br>This bit is set when the FIFO contains data that was received with a parity error, framing error or break condition.                                                      | 0x0 |
| 6    | RC | TEMT     | Transmitter Empty<br>This bit is set when the transmitter shift register is empty, it will clear as soon as data is written to the <b>TBR</b> register.                                                                                 | 0x1 |
| 5    | RC | THRE     | Transmitter Holding Register Empty<br>This bit is set when the transmitter holding register is empty, it will clear as soon as data is written to the <b>TBR</b> register.                                                              | 0x1 |
| 4    | RC | BI       | Break Interrupt<br>This bit is set if a break is received, that is when the RXD signal is at a low state for more than one character transmission time (from start bit to stop bit). Under this condition, a single 'zero' is received. | 0x0 |
| 3    | RC | FE       | Framing Error<br>This bit is set if a valid stop bit is not detected. If a framing error occurs, the receiver will attempt to re-synchronize by sampling the Start Bit twice and then takes the data.                                   | 0x0 |
| 2    | RC | PE       | Parity Error<br>This bit is set if the received parity is different from the expected value.                                                                                                                                            | 0x0 |
| 1    | RC | OE       | Overrun Error<br>This bit is set when a receive overrun occurs. This will happen if a character is received before the previous character has been read by firmware.                                                                    | 0x0 |
| 0    | RC | DR       | Data Ready<br>This bit is set when a character is received, and has been transferred in to the receiver buffer register. This bit will reset when all the characters are read from the receiver buffer register.                        | 0x0 |

MSR : Modem Status Register (offset: 0x0020)

| Bits | Type | Name | Description                                                                                       | Initial value |
|------|------|------|---------------------------------------------------------------------------------------------------|---------------|
| 31:8 | -    | -    | Reserved                                                                                          | 0x0           |
| 7    | RC   | DCD  | Data Carrier Detect<br>This bit is set when the DCDN (Data Carrier Detect) pin is at a low value. | 0x0           |
| 6    | RC   | RI   | Ring Indicator<br>This bit is set when the RIN (Ring Indicator) pin is at a low value.            | 0x1           |
| 5    | RC   | DSR  | Data Set Ready<br>This bit is set when the DSRN (Data Set Ready) pin is at a low value.           | 0x0           |
| 4    | RC   | CTS  | Clear to Send<br>This bit is set when the CTSN (Clear to Send) pin is at a low value.             | 0x0           |
| 3    | RC   | DDCD | Delta Data Carrier Detect<br>This bit is set when the DCDN (Data Carrier Detect) pin changes.     | 0x0           |
| 2    | RC   | TERI | Trailing Edge Ring Indicator<br>This bit is set when the RIN (Ring Indicator) pin changes         | 0x0           |

|   |    |      |                                                                                     |     |
|---|----|------|-------------------------------------------------------------------------------------|-----|
|   |    |      | from a low to a high value.                                                         |     |
| 1 | RC | DDSR | Delta Data Set Ready<br>This bit is set when the DSRN (Data Set Ready) pin changes. | 0x0 |
| 0 | RC | DCTS | Delta Clear to Send<br>This bit is set when the CTSN (Clear to Send) pin changes.   | 0x0 |

SCRATCH : Scratch Register (offset: 0x0024)

| Bits | Type | Name         | Description                                                                                                                                          | Initial value |
|------|------|--------------|------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:8 | -    | -            | Reserved                                                                                                                                             | 0x0           |
| 7:0  | RW   | SCRATCH[7:0] | Scratch<br>This register is defined as a scratch register in 16550 application. It has no hardware function, and is retained for compatibility only. | 0x0           |

DL : Clock Divider Divisor Latch (offset: 0x0028)

| Bits           | Type          | Name     | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | Initial value  |               |          |              |          |       |    |        |  |        |    |        |  |        |    |        |  |        |   |       |  |        |   |       |     |
|----------------|---------------|----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|---------------|----------|--------------|----------|-------|----|--------|--|--------|----|--------|--|--------|----|--------|--|--------|---|-------|--|--------|---|-------|-----|
| 31:16          | -             | -        | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | 0x0            |               |          |              |          |       |    |        |  |        |    |        |  |        |    |        |  |        |   |       |  |        |   |       |     |
| 15:0           | RW            | DL[15:0] | <div>Divisor Latch</div> <div>This register is used in the clock divider to generate the baud clock. baud rate (transfer rate in bits per second) is defined as:<br/>baud rate = 40MHz / (CLKDIV * 16).</div> <div>Note: In standard 16550 implementation, this register is accessible as two 8-bit halves only. In this implementation, the DL register is accessible as a single 16-bit entity only.</div> <div>NOTE: DL[15:0] should be &gt;= 4</div> <table><thead><tr><th>Src clock(MHz)</th><th>Req Baud rate</th><th>DL[15:0]</th><th>Err Rate (%)</th></tr></thead><tbody><tr><td>40000000</td><td>57000</td><td>44</td><td>-0.32%</td></tr><tr><td></td><td>115200</td><td>22</td><td>-1.36%</td></tr><tr><td></td><td>230400</td><td>11</td><td>-1.36%</td></tr><tr><td></td><td>345600</td><td>7</td><td>3.34%</td></tr><tr><td></td><td>460800</td><td>5</td><td>8.51%</td></tr></tbody></table> | Src clock(MHz) | Req Baud rate | DL[15:0] | Err Rate (%) | 40000000 | 57000 | 44 | -0.32% |  | 115200 | 22 | -1.36% |  | 230400 | 11 | -1.36% |  | 345600 | 7 | 3.34% |  | 460800 | 5 | 8.51% | 0x1 |
| Src clock(MHz) | Req Baud rate | DL[15:0] | Err Rate (%)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |                |               |          |              |          |       |    |        |  |        |    |        |  |        |    |        |  |        |   |       |  |        |   |       |     |
| 40000000       | 57000         | 44       | -0.32%                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |                |               |          |              |          |       |    |        |  |        |    |        |  |        |    |        |  |        |   |       |  |        |   |       |     |
|                | 115200        | 22       | -1.36%                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |                |               |          |              |          |       |    |        |  |        |    |        |  |        |    |        |  |        |   |       |  |        |   |       |     |
|                | 230400        | 11       | -1.36%                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |                |               |          |              |          |       |    |        |  |        |    |        |  |        |    |        |  |        |   |       |  |        |   |       |     |
|                | 345600        | 7        | 3.34%                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |                |               |          |              |          |       |    |        |  |        |    |        |  |        |    |        |  |        |   |       |  |        |   |       |     |
|                | 460800        | 5        | 8.51%                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |                |               |          |              |          |       |    |        |  |        |    |        |  |        |    |        |  |        |   |       |  |        |   |       |     |

DLLO : Clock Divider Divisor Latch Low (offset: 0x002c)

| Bits | Type | Name      | Description                                                                                                                                                                                                                                                                                                      | Initial value |
|------|------|-----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:8 | -    | -         | Reserved                                                                                                                                                                                                                                                                                                         | 0x0           |
| 7:0  | RW   | DLLO[7:0] | This register is the equivalent to the lower 8 bits of the DL register. It is provided for 16550 compatibility.<br>Note: In standard 16550 implementation, this register is accessible as two 8-bit halves only. For convenience, the divisor latch is accessible as a single 16-bit entity via the DL register. | 0x1           |

DLHI : Clock Divider Divisor Latch High (offset: 0x0030)

| Bits | Type | Name      | Description                                                                                                                                                                                                                                                                                         | Initial value |
|------|------|-----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:8 | -    | -         | Reserved                                                                                                                                                                                                                                                                                            | 0x0           |
| 7:0  | RW   | DLHI[7:0] | This register is the equivalent to the upper 8 bits of the DL register. It is provided for 16550 compatibility.<br>Note: In standard 16550 implementation, this register is accessible as two 8-bit halves only. For convenience, the divisor latch is accessible as a single 16-bit entity via the | 0x0           |

|  |  |  |              |  |
|--|--|--|--------------|--|
|  |  |  | DL register. |  |
|--|--|--|--------------|--|

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### 3.9 UART Lite

#### 3.9.1 Features

- 2-pin UART
- 16550-compatible register set, except for Divisor Latch register
- 5-8 data bits
- 1-2 stop bits (1 or 2 stop bits are supported with 5 data bits)
- Even, odd, stick or no parity
- All standard baud rates up to 345600 b/s
- 16-byte receive buffer
- 16-byte transmit buffer
- Receive buffer threshold interrupt
- Transmit buffer threshold interrupt
- False start bit detection in asynchronous mode
- Internal diagnostic capabilities
- Break simulation
- Loop-back control for communications link fault isolation

#### 3.9.2 Block Diagram

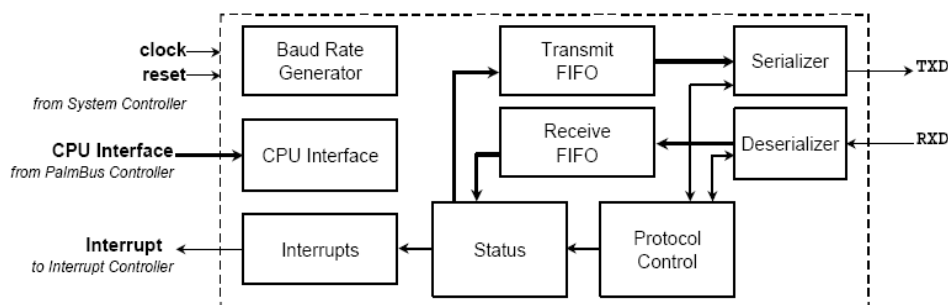


Fig. 3-8-1 UART Lite Block Diagram

#### 3.9.3 Register Description (base: 0x1000\_0c00)

RBR: Receive Buffer Register (offset: 0x0000)

| Bits | Type | Name     | Description                                                                                                                                                                                                                                                                                                        | Initial value |
|------|------|----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:8 | -    | -        | Reserved                                                                                                                                                                                                                                                                                                           | 0x0           |
| 7:0  | RO   | RXD[7:0] | Receive Buffer Data<br>Receive data. Data is transferred to this register from the receive shift register after a full character is received. The OE bit in the LSR register is set, indication a receive buffer overrun, if the contents of this register has not been read before another character is received. | 0x0           |

TBR: Transmit Buffer Register (offset: 0x0004)

| Bits | Type | Name     | Description                                                                                                                                                                                                                                             | Initial value |
|------|------|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:8 | -    | -        | Reserved                                                                                                                                                                                                                                                | 0x0           |
| 7:0  | WO   | TXD[7:0] | Transmit Buffer Data<br>Transmit data. When a character is written to this register, it is stored in the transmitter holding register; if the transmitter register is empty, the character is moved to the transmitter register, starting transmission. | 0x0           |

IER : Interrupt Enable Register (offset: 0x0008)

| Bits | Type | Name  | Description                                                                                                                                                         | Initial value |
|------|------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:3 | -    | -     | Reserved                                                                                                                                                            | 0x0           |
| 2    | RW   | ELSI  | Enable Receiver Line Status Interrupt<br>1: Enable line status (OE, PE, FE, and BI) interrupts.<br>0: Disable line status (OE, PE, FE, and BI) interrupts.          | 0x0           |
| 1    | RW   | ETBEI | Enable Transmitter Buffer Line Status Interrupt<br>1: Enable transmit buffer empty (THRE) interrupt.<br>0: Disable transmit buffer empty (THRE) interrupt.          | 0x0           |
| 0    | RW   | ERBFI | Enable Receiver Buffer Empty Interrupt<br>1: Enable data ready (DR) or character time-out interrupt.<br>0: Disable data ready (DR) or character time-out interrupt. | 0x0           |

IIR: Interrupt Identification Register (offset: 0x000c)

| Bits | Type     | Name                 | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | Initial value |          |      |        |   |  |           |  |   |  |           |  |   |  |           |  |   |  |           |  |   |   |                      |             |   |   |                      |    |   |   |                 |      |   |   |                    |                    |     |
|------|----------|----------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|----------|------|--------|---|--|-----------|--|---|--|-----------|--|---|--|-----------|--|---|--|-----------|--|---|---|----------------------|-------------|---|---|----------------------|----|---|---|-----------------|------|---|---|--------------------|--------------------|-----|
| 31:8 | -        | -                    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | 0x0           |          |      |        |   |  |           |  |   |  |           |  |   |  |           |  |   |  |           |  |   |   |                      |             |   |   |                      |    |   |   |                 |      |   |   |                    |                    |     |
| 7:6  | RO       | FIFOENA [1:0]        | FIFOs Enabled<br>FIFOs Enabled. These bits reflect the FIFO enable bit setting in the FIFO Control Register. When the FIFO enable bit is set, both of these bits will be set high to a value of '11'. When the FIFO enable bit is cleared, both of these bits will be set low to a value of '00'.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | 0x0           |          |      |        |   |  |           |  |   |  |           |  |   |  |           |  |   |  |           |  |   |   |                      |             |   |   |                      |    |   |   |                 |      |   |   |                    |                    |     |
| 5:4  | -        | -                    | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | 0x0           |          |      |        |   |  |           |  |   |  |           |  |   |  |           |  |   |  |           |  |   |   |                      |             |   |   |                      |    |   |   |                 |      |   |   |                    |                    |     |
| 3:1  | RO       | INTID[2:0]           | <div>Interrupt Identifier<br/>Interrupt ID. These bits provide a snapshot of the interrupt type, and may be used as the offset into an interrupt vector table. The interrupt encoding is given below.</div> <table><tr><th>ID</th><th>Priority</th><th>Type</th><th>Source</th></tr><tr><td>7</td><td></td><td>Undefined</td><td></td></tr><tr><td>6</td><td></td><td>Undefined</td><td></td></tr><tr><td>5</td><td></td><td>Undefined</td><td></td></tr><tr><td>4</td><td></td><td>Undefined</td><td></td></tr><tr><td>3</td><td>1</td><td>Receiver Line Status</td><td>OE,PE,FE,BI</td></tr><tr><td>2</td><td>2</td><td>Receiver Buffer Full</td><td>DR</td></tr><tr><td>1</td><td>3</td><td>Transmit buffer</td><td>THRE</td></tr><tr><td>0</td><td>4</td><td>Empty Modem Status</td><td>DCTD,DDSR, RI, DCD</td></tr></table> <div>If more than one category of interrupt is asserted, only the highest priority ID will be given. The line and Modem status interrupts are cleared by reading the corresponding status register (LSR, MSR). The Receive Buffer Full interrupt will be cleared when all of the data is read from the receiver buffer. The Transmitter Buffer empty will be cleared when data is written to the TBR register.<br/>See also "Interrupt Priorities".</div> | ID            | Priority | Type | Source | 7 |  | Undefined |  | 6 |  | Undefined |  | 5 |  | Undefined |  | 4 |  | Undefined |  | 3 | 1 | Receiver Line Status | OE,PE,FE,BI | 2 | 2 | Receiver Buffer Full | DR | 1 | 3 | Transmit buffer | THRE | 0 | 4 | Empty Modem Status | DCTD,DDSR, RI, DCD | 0x0 |
| ID   | Priority | Type                 | Source                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |               |          |      |        |   |  |           |  |   |  |           |  |   |  |           |  |   |  |           |  |   |   |                      |             |   |   |                      |    |   |   |                 |      |   |   |                    |                    |     |
| 7    |          | Undefined            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |               |          |      |        |   |  |           |  |   |  |           |  |   |  |           |  |   |  |           |  |   |   |                      |             |   |   |                      |    |   |   |                 |      |   |   |                    |                    |     |
| 6    |          | Undefined            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |               |          |      |        |   |  |           |  |   |  |           |  |   |  |           |  |   |  |           |  |   |   |                      |             |   |   |                      |    |   |   |                 |      |   |   |                    |                    |     |
| 5    |          | Undefined            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |               |          |      |        |   |  |           |  |   |  |           |  |   |  |           |  |   |  |           |  |   |   |                      |             |   |   |                      |    |   |   |                 |      |   |   |                    |                    |     |
| 4    |          | Undefined            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |               |          |      |        |   |  |           |  |   |  |           |  |   |  |           |  |   |  |           |  |   |   |                      |             |   |   |                      |    |   |   |                 |      |   |   |                    |                    |     |
| 3    | 1        | Receiver Line Status | OE,PE,FE,BI                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |               |          |      |        |   |  |           |  |   |  |           |  |   |  |           |  |   |  |           |  |   |   |                      |             |   |   |                      |    |   |   |                 |      |   |   |                    |                    |     |
| 2    | 2        | Receiver Buffer Full | DR                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |               |          |      |        |   |  |           |  |   |  |           |  |   |  |           |  |   |  |           |  |   |   |                      |             |   |   |                      |    |   |   |                 |      |   |   |                    |                    |     |
| 1    | 3        | Transmit buffer      | THRE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |               |          |      |        |   |  |           |  |   |  |           |  |   |  |           |  |   |  |           |  |   |   |                      |             |   |   |                      |    |   |   |                 |      |   |   |                    |                    |     |
| 0    | 4        | Empty Modem Status   | DCTD,DDSR, RI, DCD                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |               |          |      |        |   |  |           |  |   |  |           |  |   |  |           |  |   |  |           |  |   |   |                      |             |   |   |                      |    |   |   |                 |      |   |   |                    |                    |     |
| 0    | RO       | INTPEND              | Interrupt Pending<br>0: An interrupt bit is set and is not masked.<br>1: No interrupts are pending.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | RS            |          |      |        |   |  |           |  |   |  |           |  |   |  |           |  |   |  |           |  |   |   |                      |             |   |   |                      |    |   |   |                 |      |   |   |                    |                    |     |

FCR: FIFO Control Register (offset: 0x0010)

| Bits | Type | Name         | Description                                                                                                                                                                                                 | Initial value |
|------|------|--------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:8 | -    | -            | Reserved                                                                                                                                                                                                    | 0x0           |
| 7:6  | RW   | RXTRIG [1:0] | Receiver Trigger Level<br>The data ready interrupt (DR) will be asserted when the receiver buffer depth is equal to the number of characters programmed in the trigger register. The trigger level encoding | 0x0           |



|        |               |             | is as follows:                                                                                                                                                                                                                                                                                                                                                                                                         |        |               |   |   |   |   |   |   |   |    |     |
|--------|---------------|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|---------------|---|---|---|---|---|---|---|----|-----|
|        |               |             | <table><tr><th>RXTRIG</th><th>Trigger Level</th></tr><tr><td>0</td><td>1</td></tr><tr><td>1</td><td>4</td></tr><tr><td>2</td><td>8</td></tr><tr><td>3</td><td>14</td></tr></table>                                                                                                                                                                                                                                     | RXTRIG | Trigger Level | 0 | 1 | 1 | 4 | 2 | 8 | 3 | 14 |     |
| RXTRIG | Trigger Level |             |                                                                                                                                                                                                                                                                                                                                                                                                                        |        |               |   |   |   |   |   |   |   |    |     |
| 0      | 1             |             |                                                                                                                                                                                                                                                                                                                                                                                                                        |        |               |   |   |   |   |   |   |   |    |     |
| 1      | 4             |             |                                                                                                                                                                                                                                                                                                                                                                                                                        |        |               |   |   |   |   |   |   |   |    |     |
| 2      | 8             |             |                                                                                                                                                                                                                                                                                                                                                                                                                        |        |               |   |   |   |   |   |   |   |    |     |
| 3      | 14            |             |                                                                                                                                                                                                                                                                                                                                                                                                                        |        |               |   |   |   |   |   |   |   |    |     |
|        |               |             | Note: This register is not used if the receive FIFO is disabled.                                                                                                                                                                                                                                                                                                                                                       |        |               |   |   |   |   |   |   |   |    |     |
| 5:4    | RW            | TXTRIG[1:0] | Transmitter Trigger Level<br>The THRE interrupt will be asserted if the transmitter buffer depth is less than or equal to the number of characters programmed in the trigger register. The trigger level encoding is as follows:<br><table><tr><th>TXTRIG</th><th>Trigger Level</th></tr><tr><td>0</td><td>1</td></tr><tr><td>1</td><td>4</td></tr><tr><td>2</td><td>8</td></tr><tr><td>3</td><td>12</td></tr></table> | TXTRIG | Trigger Level | 0 | 1 | 1 | 4 | 2 | 8 | 3 | 12 | 0x0 |
| TXTRIG | Trigger Level |             |                                                                                                                                                                                                                                                                                                                                                                                                                        |        |               |   |   |   |   |   |   |   |    |     |
| 0      | 1             |             |                                                                                                                                                                                                                                                                                                                                                                                                                        |        |               |   |   |   |   |   |   |   |    |     |
| 1      | 4             |             |                                                                                                                                                                                                                                                                                                                                                                                                                        |        |               |   |   |   |   |   |   |   |    |     |
| 2      | 8             |             |                                                                                                                                                                                                                                                                                                                                                                                                                        |        |               |   |   |   |   |   |   |   |    |     |
| 3      | 12            |             |                                                                                                                                                                                                                                                                                                                                                                                                                        |        |               |   |   |   |   |   |   |   |    |     |
| 3      | RW            | DMAMODE     | Enable DMA transfers<br>This bit is writeable and readable, but has no other hardware function.                                                                                                                                                                                                                                                                                                                        | 0x0    |               |   |   |   |   |   |   |   |    |     |
| 2      | RW            | TXRST       | Transmitter Reset<br>Writing a '1' to this bit will clear the transmit FIFO and reset the transmitter status. The shift register is not cleared.                                                                                                                                                                                                                                                                       | 0x0    |               |   |   |   |   |   |   |   |    |     |
| 1      | RW            | RXRST       | Receive Reset<br>Writing a '1' to this bit will clear the receive FIFO and reset the receiver status. The shift register is not cleared.                                                                                                                                                                                                                                                                               | 0x0    |               |   |   |   |   |   |   |   |    |     |
| 0      | RW            | FIFOENA     | 0: The Transmit and Receive FIFOs have the effective depth of one character.<br>1: The Transmit and Receive FIFOs are enabled.<br>Note: The FIFO status and data are automatically cleared when this bit is changed.                                                                                                                                                                                                   | 0x0    |               |   |   |   |   |   |   |   |    |     |

LCR: Line Control Register (offset: 0x0014)

| Bits | Type | Name     | Description                                                                                                                                                                                                                            | Initial value |
|------|------|----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:8 | -    | -        | Reserved                                                                                                                                                                                                                               | 0x0           |
| 7    | RW   | DLAB     | <p>Divisor Latch Access Bit</p> <p>This bit has no functionality, and is retained for compatibility only</p>                                                                                                                           | 0x0           |
| 6    | RW   | SETBRK   | <p>Set Break Condition</p> <p>0: Normal functionality.</p> <p>1: Force TXD pin to '0'. Transmitter otherwise operates normally.</p>                                                                                                    | 0x0           |
| 5    | RW   | FORCEPAR | <p>Force Parity Bit</p> <p>0: Normal functionality.</p> <p>1: If even parity is selected, the (transmitted and checked) parity is forced to '0'; if odd parity is selected, the (transmitted and checked) parity if forced to '1'.</p> | 0x0           |
| 4    | RW   | EPS      | <p>Even Parity Select</p> <p>0: Odd parity selected (checksum, including parity is '1').</p> <p>1: Even parity selected (checksum, including parity is '0').</p> <p>Note: This bit is ignored if the PEN bit is '0'.</p>               | 0x0           |
| 3    | RW   | PEN      | <p>Parity Enable</p> <p>0: Parity is not transmitted or checked.</p> <p>1: Parity is generated (transmit), and checked (receive).</p>                                                                                                  | 0x0           |
| 2    | RW   | STB      | Stop Bit Select                                                                                                                                                                                                                        | 0x0           |

|      |    |          |                                                                                                                                                                                        |     |
|------|----|----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|
|      |    |          | 0: 1 stop bit is transmitted and received.<br>1: 1.5 stop bits are transmitted and received if WLS is '0'; 2 stop bits are transmitted and received if WLS is '1', '2', or '3'.        |     |
| 1:0: | RW | WLS[1:0] | Word Length Select<br>0: Each character is 5 bits in length<br>1: Each character is 6 bits in length<br>2: Each character is 7 bits in length<br>3: Each character is 8 bits in length | 0x0 |

MCR: Modem Control Register (offset: 0x0018)

| Bits | Type | Name | Description                                                                                                                                                                              | Initial value |
|------|------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:5 | -    | -    | Reserved                                                                                                                                                                                 | 0x0           |
| 4    | RW   | LOOP | Loop-back Mode Enable<br>0: Normal Operation.<br>1: The UART is put into loop-back mode, used for self-test: The TXD pin is driven high; the TXD signal are connected to RXD internally. | 0x0           |
| 3:0  | -    | -    | Reserved                                                                                                                                                                                 | 0x0           |

LSR: Line Status Register (offset: 0x001c)

| Bits | Type | Name     | Description                                                                                                                                                                                                                             | Initial value |
|------|------|----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:8 | -    | -        | Reserved                                                                                                                                                                                                                                | 0x0           |
| 7    | RC   | ERINFIFO | The FIFO contains data which had a parity or framing error<br>This bit is set when the FIFO contains data that was received with a parity error, framing error or break condition.                                                      | 0x0           |
| 6    | RC   | TEMT     | Transmitter Empty<br>This bit is set when the transmitter shift register is empty, it will clear as soon as data is written to the <b>TBR</b> register.                                                                                 | 0x1           |
| 5    | RC   | THRE     | Transmitter Holding Register Empty<br>This bit is set when the transmitter holding register is empty, it will clear as soon as data is written to the <b>TBR</b> register.                                                              | 0x1           |
| 4    | RC   | BI       | Break Interrupt<br>This bit is set if a break is received, that is when the RXD signal is at a low state for more than one character transmission time (from start bit to stop bit). Under this condition, a single 'zero' is received. | 0x0           |
| 3    | RC   | FE       | Framing Error<br>This bit is set if a valid stop bit is not detected. If a framing error occurs, the receiver will attempt to re-synchronize by sampling the Start Bit twice and then takes the data.                                   | 0x0           |
| 2    | RC   | PE       | Parity Error<br>This bit is set if the received parity is different from the expected value.                                                                                                                                            | 0x0           |
| 1    | RC   | OE       | Overrun Error<br>This bit is set when a receive overrun occurs. This will happen if a character is received before the previous character has been read by firmware.                                                                    | 0x0           |
| 0    | RC   | DR       | Data Ready<br>This bit is set when a character is received, and has been transferred in to the receiver buffer register. This bit will reset when all the characters are read from the receiver buffer register.                        | RS            |

DL: Clock Divider Divisor Latch (offset: 0x0028)

| Bits  | Type | Name | Description | Initial value |
|-------|------|------|-------------|---------------|
| 31:16 | -    | -    | Reserved    | 0x0           |

| 15:0           | RW            | DL[15:0] | <div><div>Divisor Latch</div><div>This register is used in the clock divider to generate the baud clock. The baud rate (transfer rate in bits per second) is defined as:<br/>Baud rate = system clock frequency / (CLKDIV * 16).</div><div>Note: In standard 16550 implementation, this register is accessible as two 8-bit halves only. In this implementation, the DL register is accessible as a single 16-bit entity only.</div><div>NOTE: DL[15:0] should be &gt;= 4</div><table><thead><tr><th>Src clock(MHz)</th><th>Req Baud rate</th><th>DL[15:0]</th><th>Err Rate (%)</th></tr></thead><tbody><tr><td>40000000</td><td>57000</td><td>44</td><td>-0.32%</td></tr><tr><td></td><td>115200</td><td>22</td><td>-1.36%</td></tr><tr><td></td><td>230400</td><td>11</td><td>-1.36%</td></tr><tr><td></td><td>345600</td><td>7</td><td>3.34%</td></tr><tr><td></td><td>460800</td><td>5</td><td>8.51%</td></tr></tbody></table></div> | Src clock(MHz) | Req Baud rate | DL[15:0] | Err Rate (%) | 40000000 | 57000 | 44 | -0.32% |  | 115200 | 22 | -1.36% |  | 230400 | 11 | -1.36% |  | 345600 | 7 | 3.34% |  | 460800 | 5 | 8.51% | 0x1 |
|----------------|---------------|----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|---------------|----------|--------------|----------|-------|----|--------|--|--------|----|--------|--|--------|----|--------|--|--------|---|-------|--|--------|---|-------|-----|
| Src clock(MHz) | Req Baud rate | DL[15:0] | Err Rate (%)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |                |               |          |              |          |       |    |        |  |        |    |        |  |        |    |        |  |        |   |       |  |        |   |       |     |
| 40000000       | 57000         | 44       | -0.32%                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |                |               |          |              |          |       |    |        |  |        |    |        |  |        |    |        |  |        |   |       |  |        |   |       |     |
|                | 115200        | 22       | -1.36%                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |                |               |          |              |          |       |    |        |  |        |    |        |  |        |    |        |  |        |   |       |  |        |   |       |     |
|                | 230400        | 11       | -1.36%                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |                |               |          |              |          |       |    |        |  |        |    |        |  |        |    |        |  |        |   |       |  |        |   |       |     |
|                | 345600        | 7        | 3.34%                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |                |               |          |              |          |       |    |        |  |        |    |        |  |        |    |        |  |        |   |       |  |        |   |       |     |
|                | 460800        | 5        | 8.51%                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |                |               |          |              |          |       |    |        |  |        |    |        |  |        |    |        |  |        |   |       |  |        |   |       |     |

DLLO: Clock Divider Divisor Latch Low (offset: 0x002c)

| Bits | Type | Name      | Description                                                                                                                                                                                                                                                                                                                   | Initial value |
|------|------|-----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:8 | -    | -         | Reserved                                                                                                                                                                                                                                                                                                                      | 0x0           |
| 7:0  | RW   | DLLO[7:0] | <p>This register is the equivalent to the lower 8 bits of the DL register. It is provided for 16550 compatibility.</p> <p>Note: In a standard 16550 implementation, this register is accessible as two 8-bit halves only. For convenience, the divisor latch is accessible as a single 16-bit entity via the DL register.</p> | 0x1           |

DLHI : Clock Divider Divisor Latch High (offset: 0x0030)

| Bits | Type | Name      | Description                                                                                                                                                                                                                                                                                                                   | Initial value |
|------|------|-----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:8 | -    | -         | Reserved                                                                                                                                                                                                                                                                                                                      | 0x0           |
| 7:0  | RW   | DLHI[7:0] | <p>This register is the equivalent to the upper 8 bits of the DL register. It is provided for 16550 compatibility.</p> <p>Note: In a standard 16550 implementation, this register is accessible as two 8-bit halves only. For convenience, the divisor latch is accessible as a single 16-bit entity via the DL register.</p> | 0x0           |

IFCTL : Interface Control (offset: 0x0034)

| Bits | Type | Name  | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                     | Initial value |
|------|------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:1 | -    | -     | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                        | 0x0           |
| 0    | RW   | IFCTL | <p>Open Collector Mode Control. This register controls if the UART Lite TXD output functions in open collector mode or is always driven. When set to '0', the output is always driven with the value of the transmit data signal. When set to a '1', the TXD output functions in open collector mode, where the TXD output is either driven low (when the transmit data output is active low) or tri-stated (when the transmit data output is active high).</p> | 0x0           |

(The remainder of this page is left blank intentionally)

### 3.10 Programmable I/O

#### 3.10.1 Features

- Support 28 programmable I/Os
- Parameterized numbers of independent inputs, outputs, and inputs
- Independent polarity controls for each pin
- Independently masked edge detect interrupt on any input transition
- Programmable I/O pins are shared pin with JTAG, UART-Lite, UART, SPI, PCM, I2C, EPHY\_LED

#### 3.10.2 Block Diagram

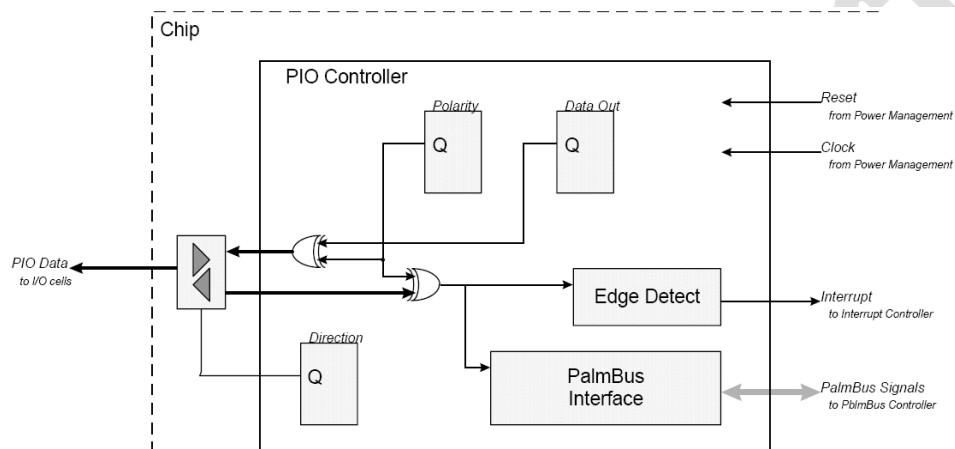


Fig. 3-9-1 Program I/O Block Diagram

#### 3.10.3 Register Description (base: 0x1000\_0600)

GPIO21\_00\_INT: Programmed I/O Interrupt Status (offset: 0x0000)

| Bits  | Type | Name         | Description                                                                                                                                                                                                                                                                                                                                                                                     | Initial value |
|-------|------|--------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:22 | -    | -            | Reserved                                                                                                                                                                                                                                                                                                                                                                                        | 0x0           |
| 21:0  | RC   | PIOINT[21:0] | A PIOINT bit is set when its corresponding PIO pin changes value and the edge for that pin is enabled via the PIORMSK or PIOFMSK register. A pin must be set as an input in the PIODIR register to generate an interrupt. All bits are cleared by writing "1" to either this register or the PIOEDGE register.<br>Note: Changes to the PIO pins can only be detected when the clock is running. | 0x0           |

GPIO21\_00\_EDGE: Programmed I/O Edge Status (offset: 0x0004)

| Bits  | Type | Name          | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | Initial value |
|-------|------|---------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:22 | -    | -             | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | 0x0           |
| 21:0  | RC   | PIOEDGE[21:0] | The PIOEDGE bits have different meanings depending on whether the interrupt for that pin is enabled via the PIORMSK or PIOFMSK register. If the interrupt is enabled, upon getting an interrupt condition (the corresponding PIOINT bit will be set), the PIOEDGE bit will be '1' if a rising edge triggered the interrupt, or '0' if a falling edge triggered the interrupt. If the interrupt is masked (disabled), the PIOEDGE bit will be set on either a rising or falling edge and remain set until cleared by firmware. Bits corresponding to pins that are not set as inputs will never be set. All bits are cleared by writing "1" to either this register or the | RS            |

|  |  |  |                                                                                                   |  |
|--|--|--|---------------------------------------------------------------------------------------------------|--|
|  |  |  | PIOINT register.<br>Note: Changes to the PIO pins can only be detected when the clock is running. |  |
|--|--|--|---------------------------------------------------------------------------------------------------|--|

GPIO21\_00\_RENA: Programmed I/O Rising Edge Interrupt Enable (offset: 0x0008)

| Bits  | Type | Name          | Description                                                                                                                                                                                                                                                                                                                                                                                                                  | Initial value |
|-------|------|---------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:22 | -    | -             | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                     | 0x0           |
| 21:0  | RW   | PIORENA[21:0] | Rising edge mask for individual Programmed I/O pin<br>The bits in this register enable the PIO interrupt to be set when the data on the corresponding PIO pin transitions from a '0' to a '1', i.e. a rising edge. A '1' will allow the interrupt to be set; a '0' will not allow the interrupt so that it will not be set.<br>Note: Edge detection is done after the polarity is adjusted according to the PIOPOL register. | 0x0           |

GPIO21\_00\_FENA: Programmed I/O Falling Edge Interrupt Enable (offset: 0x000c)

| Bits  | Type | Name            | Description                                                                                                                                                                                                                                                                                                                                                                                                                    | Initial value |
|-------|------|-----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:22 | -    | -               | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                       | 0x0           |
| 21:0  | RW   | PIOFMASK [21:0] | Falling edge mask for individual Programmed I/O pin<br>The bits in this register enable the PIO interrupt to be set when the data on the corresponding PIO pin transitions from a '1' to a '0', i.e. a falling edge. A '1' will allow the interrupt to be set; a '0' will not allow the interrupt so that it will not be set.<br>Note: Edge detection is done after the polarity is adjusted according to the PIOPOL register. | 0x0           |

GPIO21\_00\_DATA: Programmed I/O Data (offset: 0x0020)

| Bits  | Type | Name          | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | Initial value |
|-------|------|---------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:22 | -    | -             | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | 0x0           |
| 21:0  | RW   | PIODATA[21:0] | Data Pin for Program I/O<br>These bits are used for driving or sensing static signals on the PIO pins. To drive a value onto a PIO pin, the corresponding bit in the PIODIR register must be set. If the corresponding direction bit is set, the value written to the bit in the PIODATA register will be driven at the pin. A read of this register returns the value of the signals currently on the PIO pins.<br>Note: The value of any bit in this register will be inverted with respect to the pin if the corresponding bit in the PIOPOL register is set, both in input and output modes.<br>Note: The values read from the PIO pins are not synchronized; the user should be sure that the data will not be changing when this register is read, or should be aware that the bits which are not static at that time may be inaccurate. | RS            |

GPIO21\_00\_DIR: Programmed I/O Direction (offset: 0x0024)

| Bits  | Type | Name         | Description                                                                                                                                                                                                                                                                                                                                              | Initial value |
|-------|------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:22 | -    | -            | Reserved                                                                                                                                                                                                                                                                                                                                                 | 0x0           |
| 21:0  | RW   | PIODIR[21:0] | Program I/O Pin Direction<br>These bits are used for selecting the data direction of the PIO pins. To configure any pin as an output, the corresponding bit should be set to '1'; to configure any pin as an input, the corresponding bit should be set to '0'. The value driven onto the PIO pins, are controlled by the PIOPOL, and PIODATA registers. | 0x0           |

GPIO21\_00\_POL: Programmed I/O Pin Polarity (offset: 0x0028)

| Bits  | Type | Name         | Description                                                                                                                                                                                                                                                                                                                                                 | Initial value |
|-------|------|--------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:22 | -    | -            | Reserved                                                                                                                                                                                                                                                                                                                                                    | 0x0           |
| 21:0  | RW   | PIOPOL[21:0] | <p>Program I/O Pin Polarity</p> <p>These bits are used for controlling the polarity of the data driven on or read from the PIO pins. To invert the polarity of the data at any PIO pin, the corresponding bit should be set to '1'; a value of '0' will not modify the pin data.</p> <p>Note: The polarity controls affect both input and output modes.</p> | 0x0           |

GPIO21\_00\_SET: Set PIO Data Bit (offset: 0x002c)

| Bits  | Type | Name         | Description                                                                                                                                                                          | Initial value |
|-------|------|--------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:22 | -    | -            | Reserved                                                                                                                                                                             | 0x0           |
| 21:0  | RC   | PIOSET[21:0] | <p>These bits are used for setting bits in the PIODATA output register. Writing a '1' will set the corresponding bit in the PIODATA register. Writing a '0' will have no effect.</p> | 0x0           |

GPIO21\_00\_RESET: Clear PIO Data bit (offset: 0x0030)

| Bits  | Type | Name           | Description                                                                                                                                                                             | Initial value |
|-------|------|----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:22 | -    | -              | Reserved                                                                                                                                                                                | 0x0           |
| 21:0  | RC   | PIORESET[21:0] | <p>These bits are used for clearing bits in the PIODATA output register. Writing a '1' will clear the corresponding bit in the PIODATA register. Writing a '0' will have no effect.</p> | 0x0           |

GPIO21\_00\_TOG: Toggle PIO Data bit (offset: 0x0034)

| Bits  | Type | Name         | Description                                                                                                                                                                              | Initial value |
|-------|------|--------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:22 | -    | -            | Reserved                                                                                                                                                                                 | 0x0           |
| 21:0  | RC   | PIOTOG[21:0] | <p>These bits are used for toggling bits in the PIODATA output register. Writing a '1' will invert the corresponding bit in the PIODATA register. Writing a '0' will have no effect.</p> | RS            |

GPIO27\_22\_INT : Program I/O Interrupt Status (offset: 0x0060)

| Bits | Type | Name        | Description                                                                                                                                                                                                                                                                                                                                                                                                | Initial value |
|------|------|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 5:0  | RC   | PIOINT[5:0] | <p>A PIOINT bit is set when its corresponding PIO pin changes value and the edge for that pin is enabled via the PIORMSK or PIOFMSK register. A pin must be set as an input in the PIODIR register to generate an interrupt. All bits are cleared by writing "1" to either this register or the PIOEDGE register.</p> <p>Note: Changes to the PIO pins can only be detected when the clock is running.</p> | 0x0           |

GPIO27\_22\_EDGE : Program I/O Edge Status (offset: 0x0064)

| Bits | Type | Name         | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | Initial value |
|------|------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 5:0  | RC   | PIOEDGE[5:0] | <p>The PIOEDGE bits have different meanings depending on whether the interrupt for that pin is enabled via the PIORMSK or PIOFMSK register. If the interrupt is enabled, upon getting an interrupt condition (the corresponding PIOINT bit will be set), the PIOEDGE bit will be '1' if a rising edge triggered the interrupt, or '0' if a falling edge triggered the interrupt. If the interrupt is masked (disabled), the PIOEDGE bit will be set on either a rising or falling edge and remain set until cleared by firmware. Bits corresponding to pins that are not set as inputs will never be set. All bits are cleared by writing "1" to either this register or the PIOINT register.</p> <p>Note: Changes to the PIO pins can only be detected when the</p> | RS            |

|  |  |  |                   |  |
|--|--|--|-------------------|--|
|  |  |  | clock is running. |  |
|--|--|--|-------------------|--|

**GPIO27\_22\_RENA : Program I/O Rising Edge Interrupt Enable (offset: 0x0068)**

| Bits | Type | Name         | Description                                                                                                                                                                                                                                                                                                                                                                                                                             | Initial value |
|------|------|--------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 5:0  | RW   | PIORENA[5:0] | <p>Rising edge mask for individual Programmed I/O pin</p> <p>The bits in this register enable the PIO interrupt to be set when the data on the corresponding PIO pin transitions from a '0' to a '1', i.e. a rising edge. A '1' will allow the interrupt to be set; a '0' will not allow the interrupt so that it will not be set.</p> <p>Note: Edge detection is done after polarity is adjusted according to the PIOPOL register.</p> | 0x0           |

**GPIO27\_22\_FENA : Program I/O Falling Edge Interrupt Enable (offset: 0x006c)**

| Bits | Type | Name         | Description                                                                                                                                                                                                                                                                                                                                                                                                                               | Initial value |
|------|------|--------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 5:0  | RW   | PIORENA[5:0] | <p>Falling edge mask for individual Programmed I/O pin</p> <p>The bits in this register enable the PIO interrupt to be set when the data on the corresponding PIO pin transitions from a '1' to a '0', i.e. a falling edge. A '1' will allow the interrupt to be set; a '0' will not allow the interrupt so that it will not be set.</p> <p>Note: Edge detection is done after polarity is adjusted according to the PIOPOL register.</p> | 0x0           |

**GPIO27\_22\_DATA : Program I/O Data (offset: 0x0070 )**

| Bits | Type | Name         | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | Initial value |
|------|------|--------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 5:0  | RW   | PIODATA[5:0] | <p>Data Pin for Program I/O</p> <p>These bits are used for driving or sensing static signals on the PIO pins. To drive a value onto a PIO pin, the corresponding bit in the PIODIR register must be set. If the corresponding direction bit is set, the value written to the bit in the PIODATA register will be driven at the pin. A read of this register returns the value of the signals currently on the PIO pins.</p> <p>Note: The value of any bit in this register will be inverted with respect to the pin if the corresponding bit in the PIOPOL register is set, both in input and output modes.</p> <p>Note: The values read from the PIO pins are not synchronized; the user should be sure that the data will not be changing when this register is read, or should be aware that the bits which are not static at that time may be inaccurate.</p> | RS            |

**GPIO27\_22\_DIR : Program I/O Direction (offset: 0x0074)**

| Bits | Type | Name         | Description                                                                                                                                                                                                                                                                                                                                                         | Initial value |
|------|------|--------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 5:0  | RW   | PIODIR [5:0] | <p>Program I/O Pin Direction</p> <p>These bits are used for selecting the data direction of the PIO pins. To configure any pin as an output, the corresponding bit should be set to '1'; to configure any pin as an input, the corresponding bit should be set to '0'. The value driven onto the PIO pins, are controlled by the PIOPOL, and PIODATA registers.</p> | 0x0           |

**GPIO27\_22\_POL : Program I/O Pin Polarity(offset: 0x0078)**

| Bits | Type | Name         | Description                                                                                                                                                                                                                                                                                                                                             | Initial value |
|------|------|--------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 5:0  | RW   | PIOPOL [5:0] | <p>Program I/O Pin Polarity</p> <p>These bits are used for controlling the polarity of the data driven on or read from the PIO pins. To invert the polarity of the data at PIO pin, the corresponding bit should be set to '1'; a value of '0' will not modify the pin data.</p> <p>Note: The polarity controls affect both input and output modes.</p> | 0x0           |



GPIO27\_22\_SET : Set PIO Data Bit (offset: 0x007c)

| Bits | Type | Name         | Description                                                                                                                                                                      | Initial value |
|------|------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 5:0  | RC   | PIOSET [5:0] | These bits are used for clearing bits in the PIODATA output register. Writing a '1' will clear the corresponding bit in the PIODATA register. Writing a '0' will have no effect. | 0x0           |

GPIO27\_22\_RESET : Clear PIO Data bit (offset: 0x0080)

| Bits | Type | Name           | Description                                                                                                                                                                   | Initial value |
|------|------|----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 5:0  | RC   | PIORESET [5:0] | These bits are used for setting bits in the PIODATA output register. Writing a '1' will set the corresponding bit in the PIODATA register. Writing a '0' will have no effect. | 0x0           |

GPIO27\_22\_TOG : Toggle PIO Data bit (offset: 0x0084)

| Bits | Type | Name         | Description                                                                                                                                                                       | Initial value |
|------|------|--------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 5:0  | RC   | PIOTOG [5:0] | These bits are used for toggling bits in the PIODATA output register. Writing a '1' will invert the corresponding bit in the PIODATA register. Writing a '0' will have no effect. | RS            |

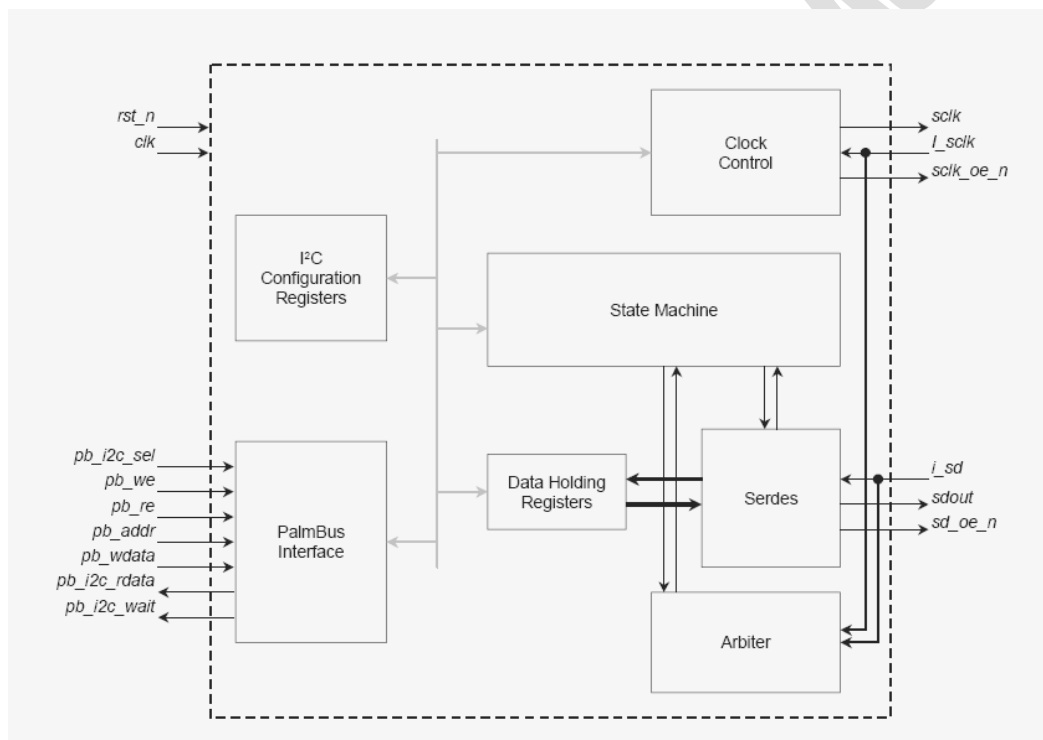


### 3.11 I2C Controller

#### 3.11.1 Features

- Two I2C Host Controllers
- Programmable I2C bus clock rate
- Supports the Synchronous Inter Integrated Circuits (I2C) serial protocol
- Bi-directional data transfer
- Programmable address width up to 8 bits
- Sequential byte read or write capability
- Device address and data address can be transmitted for device, page and address selection
- Supports Standard mode and Fast mode

#### 3.11.2 Block Diagram



#### 3.11.3 Register Description (base: 0x1000\_0900)

CONFIG: I2C Configuration Register (offset: 0x0000)

| Bits | Type | Name           | Description                                                                                                                                                                                                                 | Initial value |
|------|------|----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:8 | -    | -              | Reserved                                                                                                                                                                                                                    | 0x0           |
| 7:5  | RW   | ADDRLLEN [2:0] | Address Length<br>The value written to this register plus one will indicate the number of address bits to be transferred from the I2C <b>ADDR</b> register. Program '0' for a 1-bit address, '1' for a 2-bit address, etc.) | 0x0           |
| 4:2  | RW   | DEVADLEN [2:0] | Device Address Length<br>The value written to this register plus one indicates the number of device address bits to be transferred from the <b>DEVADDR</b> register. This field should be programmed to '6' for             | 0x0           |

|   |    |          |                                                                                                                                                                                                                                                                                                                                                   |     |
|---|----|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|
|   |    |          | compliance with I2C bus protocol.                                                                                                                                                                                                                                                                                                                 |     |
| 1 | RW | ADDRDIS  | 0: Normal transfers will occur with the address being Transmitted, followed by read or write data.<br>1: The controller will read or write serial data without transferring the address.                                                                                                                                                          | 0x0 |
| 0 | RW | DEVADDIS | 0: The device address will be transmitted before the data address.<br>1: The controller will not transfer the device address.<br>Note: if this bit is set, the ADDRDIS bit is ignored, and an address is always transmitted.<br>Note: most I2C slave devices require a device address to be transmitted; this bit should typically be set to '0'. | 0x0 |

**CLKDIV: I2C Clock Divisor Register (offset: 0x0004)**

| Bits  | Type | Name         | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | Initial value |
|-------|------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:16 | -    | -            | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | 0x0           |
| 15:0  | RW   | CLKDIV[15:0] | Clock Divisor<br>The value written to this register is used to generate the I2C bus SCLK signal by applying the following equation:<br>$SCLK\ frequency = 40MHz / (2 \times CLKDIV)$<br>Note: Only values of 8 and above are valid.<br>Note: Due to synchronization between the I2C internal clock and the system clock, the exact equation is actually<br>$SCLK\ frequency = pb\_clk\ frequency / ((2 \times CLKDIV) + 5)$ .<br>For most systems, CLKDIV is usually programmed to very larger numbers since the system clock frequency should be orders of magnitude faster than the I2C bus clock. These results in the synchronization errors being insignificant and the exact equation approximating the simpler one given above. | 0x0           |

**DEVADDR: I2C Device Address Register (offset: 0x0008)**

| Bits | Type | Name         | Description                                                                                                                                    | Initial value |
|------|------|--------------|------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:7 | -    | -            | Reserved                                                                                                                                       | 0x0           |
| 6:0  | RW   | DEVADDR[6:0] | I2C Device Address<br>This value is transmitted as the device address, if <b>DEVADDIS</b> bit in the <b>CONFIG</b> register is not set to '1'. | 0x0           |

**ADDR: I2C Address Register (offset: 0x000c)**

| Bits | Type | Name      | Description                                                                                                                            | Initial value |
|------|------|-----------|----------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:8 | -    | -         | Reserved                                                                                                                               | 0x0           |
| 7:0  | RW   | ADDR[7:0] | I2C Address<br>These bits store the 8-bits of address to be sent to the external I2C slave devices when the <b>ADDRDIS</b> bit is '0'. | 0x0           |

**DATAOUT: I2C Data Out Register (offset: 0x0010)**

| Bits | Type | Name          | Description                                                                                                                  | Initial value |
|------|------|---------------|------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:8 | -    | -             | Reserved                                                                                                                     | 0x0           |
| 7:0  | RW   | DATAOUT [7:0] | I2C Data Out<br>These bits store the 8-bits of data to be written to the external I2C slave devices during a write transfer. | 0x0           |

**DATAIN: I2C Data In Register (offset: 0x0014)**

| Bits | Type | Name | Description | Initial value |
|------|------|------|-------------|---------------|
| 31:8 | -    | -    | Reserved    | 0x0           |

|     |    |             |                                                                                                                                                                                                                                    |     |
|-----|----|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|
| 7:0 | RO | DATAIN[7:0] | I2C Data In<br>These bits store the 8-bits of data received from the external I2C slave devices during a read transaction. The <b>DATARDY</b> bit in the <b>STATUS</b> register is set to '1' when data is valid in this register. | 0x0 |
|-----|----|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|

STATUS: I2C Status Register (offset: 0x0018)

| Bits | Type | Name     | Description                                                                                                                                                                                                                                                                                                                                                           | Initial value |
|------|------|----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:5 | -    | -        | Reserved                                                                                                                                                                                                                                                                                                                                                              | 0x0           |
| 4    | RO   | STARTERR | Start Overflow Error<br>This bit is set when the <b>STARTXFR</b> register is written and a transfer is in progress. When this occurs, the write to the <b>STARTXFR</b> register is ignored. This bit is automatically cleared if firmware writes to the <b>STARTXFR</b> register when the <b>BUSY</b> bit cleared.                                                    | 0x0           |
| 3    | RO   | ACKERR   | I2C Acknowledge Error Detect<br>This bit is set when the Host controller did not receive a proper acknowledge from the I2C slave device after the transmission of a device address, address, or data out. This bit is automatically cleared when firmware writes to the <b>STARTXFR</b> register.                                                                     | 0x0           |
| 2    | RO   | DATARDY  | I2C Data Ready for Read<br>This bit indicates that the receive buffer contains valid data. It is set when data is received from an I2C slave device and is transferred from the interface shift register to the <b>DATAIN</b> register. This bit is automatically cleared when firmware reads the <b>DATAIN</b> register.                                             | 0x0           |
| 1    | RO   | SDOEMPTY | I2C Serial Data Out Register Empty<br>This bit indicates that the transmit data buffer is empty. It is cleared when the <b>DATAOUT</b> register is written to by software, and set to '1' when transmit data is transferred from the <b>DATAOUT</b> register to the interface shift register. Firmware may write to the <b>DATAOUT</b> register when this bit is '1'. | 0x1           |
| 0    | RO   | BUSY     | I2C State Machine Busy<br>This bit is '1' when the I2C interface is active, and '0' when it is idle. Firmware may initiate an I2C transfer when this bit is '0', and should not modify any I2C host controller registers while it is '1'.                                                                                                                             | 0x0           |

STARTXFR: I2C Transfer Start Register (offset: 0x001c)

| Bits | Type | Name    | Description                                                                                    | Initial value |
|------|------|---------|------------------------------------------------------------------------------------------------|---------------|
| 31:3 | -    | -       | Reserved                                                                                       | 0x0           |
| 2    | RW   | NO_STOP | Initiate transfer without STOP.<br>It is applied to generate the SR(Start Repeat) transaction. | 0x0           |

|   |    |        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |     |
|---|----|--------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|
| 1 | RW | NODATA | Initiate transfer without transferring data<br>When this register is written with this bit set, an address-only transaction is initiated. If <b>DEVADDIS</b> is '0', the device address, direction, address and stop condition are transmitted to the I2C slave device. If <b>DEVADDIS</b> is '1', the address and stop condition are transmitted to the I2C slave device. This bit should be written with a '0' for normal I2C bus accesses.<br>Note: <b>ADDRDIS</b> is ignored if this bit is set for a transaction. | 0x0 |
| 0 | RW | RWDIR  | Read/Write Direction<br>When this register is written with this bit set, a read transaction is initiated; when written with this bit reset, a write transaction is initiated.<br>Note: this bit is shifted out to the I2C slave device after the device address; if <b>DEVADDIS</b> is '1', this bit is not shifted out to the device.                                                                                                                                                                                 | 0x0 |

**BYTECNT: I2C Byte Counter Register (offset: 0x0020)**

| Bits | Type | Name        | Description                                                                                                                                                                                                                                                                                                                 | Initial value |
|------|------|-------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:6 | -    | -           | Reserved                                                                                                                                                                                                                                                                                                                    | 0x0           |
| 5:0  | RW   | BYTCNT[5:0] | Byte Count used for sequential reads/writes<br>The value written to this register plus one indicates the number of data bytes to be written to or read from the external I2C slave device. If its value is non-zero, multiple sequential read or write cycles will be issued with a single address (and/or device address). | 0x0           |

**Programming Description.**

Write Operation: (Single)

|   |         |      |         |      |      |      |   |
|---|---------|------|---------|------|------|------|---|
| S | DEV_ADR | A(S) | SUB_ADR | A(S) | DATA | A(S) | P |
|---|---------|------|---------|------|------|------|---|

|   |         |      |         |      |      |      |   |
|---|---------|------|---------|------|------|------|---|
| S | DEV_ADR | A(S) | SUB_ADR | A(S) | DATA | A(M) | P |
|---|---------|------|---------|------|------|------|---|

PS: the bit-width of DEV\_ADR is defined in REG(CONFIG) bit[7:5]  
the bit-width of SUB\_ADR is defined in REG(CONFIG) bit[4:2]

PS: As REG(CONFIG) bit[1]=1'b1, the SUB\_ADR field will be absent. (the waveform will be shown as below.)

|   |         |      |      |      |   |
|---|---------|------|------|------|---|
| S | DEV_ADR | A(S) | DATA | A(S) | P |
|---|---------|------|------|------|---|

PS: As REG(CONFIG) bit[0]=1'b1, the DEV\_ADR field will be absent. (the waveform will be shown as below.)

|   |         |      |      |      |   |
|---|---------|------|------|------|---|
| S | SUB_ADR | A(S) | DATA | A(S) | P |
|---|---------|------|------|------|---|

**Sequence Write Operation:**

|          |   |         |      |         |      |      |      |
|----------|---|---------|------|---------|------|------|------|
| Action-1 | S | DEV_ADR | A(S) | SUB_ADR | A(S) | DATA | A(S) |
|----------|---|---------|------|---------|------|------|------|

|          |    |         |      |      |      |   |
|----------|----|---------|------|------|------|---|
| Action-2 | RS | DEV_ADR | A(S) | DATA | A(S) | P |
|----------|----|---------|------|------|------|---|

Action-1: SET REG(STARTXFR) bit[2]=1'b1, the "STOP" <P> field will absent.  
Action-2: SET REG(STARTXFR) bit[2]=1'b0, the "STOP" <P> field will appear.

|   |           |      |                       |
|---|-----------|------|-----------------------|
| S | START bit | A(S) | ACKNOWLEDGE BY DEVICE |
| P | STOP bit  | A(M) | ACKNOWLEDGE BY HOST   |

**Initialization:**

DSR5350\_V1.0\_091408  
Form No. : QS-073-F02

Rev. : 1

Kept by : DCC

-60-  
Ret. Time : 5 Years

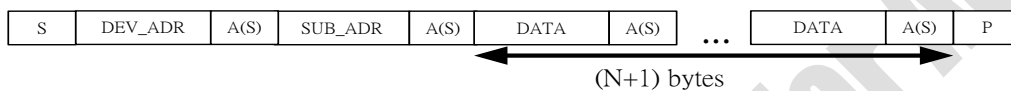
- 1) config the REG(CLKDIV) to decide the clock frequency of I2C
- 2) config the bit width of DEV\_ADDR & SUB\_ADDR by configure REG(CONFIG)

#### Read/Write Operation:

- 1) Write the DEV\_ADDR and SUB\_ADDR to REG(DEVADDR) & REG(ADDR)
- 2) Write the DATAout (REG(DATAOUT)) for write operation.
- 3) Write the operation cfg by REG(STARTXFR) to kick off the command.
- 4) Read the BUSY status by REG(STATUS) to monitor if the operation is done.
- 5) Read back the REG(DATAIN) for read operation.

#### Multiple Data Transfer: (write operation.)

E.g. we want to write (n+1) beats data by I2C



#### Burst Write Operation:

- 1) Write the DEV\_ADDR and SUB\_ADDR to REG(DEVADDR) & REG(ADDR)
- 2) Write (N) to REG(BYTECNT).
- 3) Write the REG(DATAOUT) for write operation.
- 4) Write the operation cfg by REG(STARTXFR) to kick off the command.
- 5) Read the SDOEMPTY bit by REG(STATUS) to monitor if the data is sent.
- 6) quit as all data is written, otherwise put the new data to the REG(DATAOUT) for write operation.
- 7) continue step 4.

#### Multiple Data Transfer: (read operation.)

E.g. we want to read (n+1) beats data by I2C



#### Burst Read Operation:

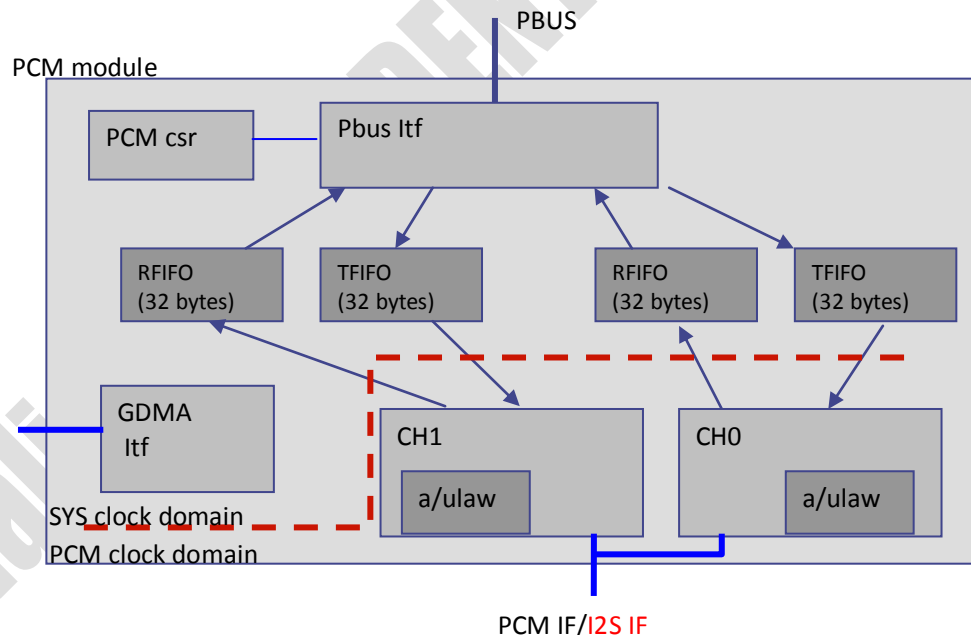
- 1) Write the DEV\_ADDR and SUB\_ADDR to REG(DEVADDR) & REG(ADDR)
- 2) Write (N) to REG(BYTECNT).
- 3) Write the operation cfg by REG(STARTXFR) to kick off the command.
- 4) Read the DATARDY bit by REG(STATUS) to monitor if the data is obtained.
- 5) Read REG(DATAIN) and continue step-4 until all bytes are read.

### 3.12 PCM Controller

#### 3.12.1 Features

- PCM module provides PBUS interface for register configuration and data transfer
- Two clock sources are reserved for PCM circuit. (From internal clock generator, int\_pcm\_clk, and from external clock source, ext\_pcm\_clk)
- PCM module can drive a clock out (with fractional-N clock divisor) to external codec.
- 2 channels PCM are available. 4~128 slots are configurable.
- Each channel supports a-law(8-bits)/u-law(8-bits)/raw-PCM(16-bits) transfer.
- Hardware converter of a-law?raw-16 and u-law ? raw-16 are implemented in design.
- Support long(8 cycle)/short(1 cycles)/configurable(interval & start point are configurable) FSYNC.
- All signals are driven by rising edge and latched by falling edge.
- Last bit of DTX will be tri-stated on falling edge.
- Begin of slot is configurable by 10 bits registers each channel.
- 32 bytes FIFO are available for each channel
- PCM interface can emulate I2S interface (16-bits data-width only).
- MSB/LSB order is configurable.
- support both of a-law/u-law(8-bits) → linear PCM(16-bits) and linear PCM(16bits) → a-law/u-law(8-bits)

#### 3.12.2 Block Diagram



Two clocks domains are partitioned in this design. PCM converter (ulaw?raw-16bit and alaw?raw-16bit) are implemented in PCM mxDmx. The threshold of FIFO is configurable. As the threshold reaches, PCM will (a) trigger the DMA interface to notify external DMA engine to transfer data. (b) trigger the interrupts to host.

The interrupt sources include :

- threshold is reached
- FIFO under run or overrun.
- fault is detected at DMA interface.

The A-law and u-law converter is implemented base on ITU-G.711 A-law and u-law table. In this design, support both of a-law/u-law(8-bits) → linear PCM(16-bits) and linear PCM(16bits) → a-law/u-law(8-bits)

The data-flow from codec to PCM-controller (RX-flow) is shown as below:

- PCM-controller latches the data from DRX at indicated time slot and then writes it to FIFO. If FIFO full, the data will be lost.
- As the RX-FIFO reach the threshold, two actions may be taken
- As DMA\_ENA=1, DMA\_REQ will be asserted to request a burst transfer. And it will re-check the FIFO threshold after DMA\_END is asserted by GDMA. (GDMA should be configured before channel is enabled.)
- Assert the Interrupt source to notify HOST. HOST can check RFIFO\_AVAIL information then get back the data from FIFO.

The data-flow from PCM-controller to codec (TX-flow) is shown as below:

- After GDMA is configured, software should configure and enable the PCM channel.
- The empty FIFO should
- As DMA\_ENA=1, DMA\_REQ will be triggered to request a burst transfer. And it will re-check the FIFO threshold after DMA\_END is asserted by GDMA (a burst is completed.).
- Assert the Interrupt source to notify HOST. HOST will write down the data to TX-FIFO. After that, HOST will recheck TFIFO\_EMPTY information then write more data if available.

NOTICE: As DMA\_ENA=1, the burst size of GDMA should less than the threshold value.

### 3.12.3 Register Description (base: 0x1000\_2000)

GLB\_CFG: GLB\_CFG Register (offset: 0x0000)

| Bits  | Type | Name      | Description                                                                                                                                                                                      | Initial value |
|-------|------|-----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31    | RW   | PCM_EN    | PCM enable,<br>1: enable<br>0: disable, all FSM and control register of PCM_mxDmx will be clear to default value.                                                                                | 0x0           |
| 30    | RW   | DMA_EN    | DMA enable<br>1: enable DMA interface, transfer data with DMA<br>0: disable DMA interface, transfer data with software.                                                                          | 0x0           |
| 29:23 | -    | -         | Reserved                                                                                                                                                                                         | 0x0           |
| 22:20 | RW   | RFF_THRES | RXFIFO threshold, As threshold reach, host/dma will be notified to fill FIFO. (unit = word)<br>It should be >2 and <6<br>As data in FIFO under the threshold, interrupt & DMA will be triggered. | 0x4           |
| 19    | -    | -         | Reserved                                                                                                                                                                                         | 0x0           |
| 18:16 | RW   | TFF_THRES | TXFIFO threshold, As threshold reach, host/dma will be notified to fill FIFO. (unit = word)<br>It should be >2 and <6.<br>As data in FIFO over the threshold, interrupt & DMA will be triggered. | 0x4           |
| 15:10 | -    | -         | Reserved                                                                                                                                                                                         | 0x0           |
| 9     | RW   | CH1-TX_EN | Channel-1 TX enable                                                                                                                                                                              | 0x0           |
| 8     | RW   | CH0-TX_EN | Channel-0 TX enable                                                                                                                                                                              | 0x0           |
| 7:2   | -    | -         | Reserved                                                                                                                                                                                         | 0x0           |
| 1     | RW   | CH1-RX_EN | Channel-1 RX enable                                                                                                                                                                              | 0x0           |
| 0     | RW   | CH0-RX_EN | Channel-0 RX enable                                                                                                                                                                              | 0x0           |

|  |  |  |                        |  |
|--|--|--|------------------------|--|
|  |  |  | 1: enable<br>0:disable |  |
|--|--|--|------------------------|--|

**PCM\_CFG: PCM\_CFG Register (offset: 0x0004)**

| Bits  | Type | Name       | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | Initial value |
|-------|------|------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31    | -    | -          | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | 0x0           |
| 30    | RW   | CLKOUT_EN  | Enable the PCM_CLK_OUT<br>1: PCM clock is provide from internal divisor.<br>0: PCM clock is provide from external Codec/OSC<br>(NOTE: Normally, the register should be asserted to '1'. And it should be asserted after divider cfg & divider clock enable)                                                                                                                                                                                                                                                       | 0x0           |
| 29:28 | -    | -          | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | 0x0           |
| 27    | RW   | EXT_FSYNC  | FSYNC is provided by external.<br>1: FSYNC is provided by external<br>0: FSYNC is generated by internal circuit.                                                                                                                                                                                                                                                                                                                                                                                                  | 0x0           |
| 26    | RW   | LONG_FSYNC | FSYNC mode:<br>1: long FSYNC<br>0: short FSYNC                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | 0x0           |
| 25    | RW   | FSYNC_POL  | Polarity of FSYNC<br>1: FSYNC is high active<br>0: FSYNC is low active                                                                                                                                                                                                                                                                                                                                                                                                                                            | 0x1           |
| 24    | RW   | DTX_TRI    | Tristate the DTX as fall edge as last bit.<br>1: Tristate the DTX<br>0: non- Tristate the DTX                                                                                                                                                                                                                                                                                                                                                                                                                     | 0x1           |
| 23:3  | -    | -          | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | 0x0           |
| 2:0   | RW   | SLOT_MODE  | How many slot each PCM frame<br>0: 4 slots, PCM clock out/in should be 256KHz.<br>1: 8 slots, PCM clock out/in should be 512KHz.<br>2:16 slots, PCM clock out/in should be 1.024MHz.<br>3:32 slots, PCM clock out/in should be 2.048MHz.<br>4:64 slots, PCM clock out/in should be 4.096MHz.<br>5:128 slots, PCM clock out/in should be 8.192MHz.<br>other: reserved.<br>Note: When using the external clock, the frequency clock should be equal to PCM_clock out. Otherwise, the PCM_CLKin should be 8.192 MHz. | 0x0           |

**INT\_STATUS: INT\_STATUS Register (offset: 0x0008)**

| Bits  | Type | Name           | Description                                                               | Initial value |
|-------|------|----------------|---------------------------------------------------------------------------|---------------|
| 31:16 | -    | -              | Reserved                                                                  | 0x0           |
| 15    | W1C  | CH1T_DMA_FAULT | Found any fault of the CH1-TX's DMA signals. (Write '1' to clear)         | 0x0           |
| 14    | W1C  | CH1T_OVRUN     | The FIFO of CH1-TX overrun(Write '1' to clear)                            | 0x0           |
| 13    | W1C  | CH1T_UNRUN     | The FIFO of CH1-TX underrun(Write '1' to clear)                           | 0x0           |
| 12    | W1C  | CH1T_THRES     | The FIFO of CH1-TX lower than the defined threshold. (Write '1' to clear) | 0x0           |
| 11    | W1C  | CH1R_DMA_FAULT | Found any fault of the CH1-RX's DMA signals. (Write '1' to clear)         | 0x0           |
| 10    | W1C  | CH1R_OVRUN     | The FIFO of CH1-RX overrun(Write '1' to clear)                            | 0x0           |
| 9     | W1C  | CH1R_UNRUN     | The FIFO of CH1-RX underrun(Write '1' to clear)                           | 0x0           |
| 8     | W1C  | CH1R_THRES     | The FIFO of CH1-RX lower than the defined threshold. (Write '1' to clear) | 0x0           |
| 7     | W1C  | CH0T_DMA_FAULT | Found any fault of the CH0-TX's DMA signals. (Write '1' to clear)         | 0x0           |



|   |     |                |                                                                           |     |
|---|-----|----------------|---------------------------------------------------------------------------|-----|
| 6 | W1C | CH0T_OVRUN     | The FIFO of CH0-TX overrun(Write '1' to clear)                            | 0x0 |
| 5 | W1C | CH0T_UNRUN     | The FIFO of CH0-TX underrun(Write '1' to clear)                           | 0x0 |
| 4 | W1C | CH0T_THRES     | The FIFO of CH0-TX lower than the defined threshold. (Write '1' to clear) | 0x0 |
| 3 | W1C | CH0R_DMA_FAULT | Found any fault of the CH0-RX's DMA signals. (Write '1' to clear)         | 0x0 |
| 2 | W1C | CH0R_OVRUN     | The FIFO of CH0-RX overrun(Write '1' to clear)                            | 0x0 |
| 1 | W1C | CH0R_UNRUN     | The FIFO of CH0-RX underrun(Write '1' to clear)                           | 0x0 |
| 0 | W1C | CH0R_THRES     | The FIFO of CH0-RX lower than the defined threshold. (Write '1' to clear) | 0x0 |

INT\_EN: INT\_EN Register (offset: 0x000c)

| Bits  | Type | Name     | Description           | Initial value |
|-------|------|----------|-----------------------|---------------|
| 31:16 | -    | -        | Reserved              | 0x0           |
| 15    | RW   | INT15_EN | Enable INT_STATUS[15] | 0x0           |
| 14    | RW   | INT14_EN | Enable INT_STATUS[14] | 0x0           |
| 13    | RW   | INT13_EN | Enable INT_STATUS[13] | 0x0           |
| 12    | RW   | INT12_EN | Enable INT_STATUS[12] | 0x0           |
| 11    | RW   | INT11_EN | Enable INT_STATUS[11] | 0x0           |
| 10    | RW   | INT10_EN | Enable INT_STATUS[10] | 0x0           |
| 9     | RW   | INT9_EN  | Enable INT_STATUS[9]  | 0x0           |
| 8     | RW   | INT8_EN  | Enable INT_STATUS[8]  | 0x0           |
| 7     | RW   | INT7_EN  | Enable INT_STATUS[7]  | 0x0           |
| 6     | RW   | INT6_EN  | Enable INT_STATUS[6]  | 0x0           |
| 5     | RW   | INT5_EN  | Enable INT_STATUS[5]  | 0x0           |
| 4     | RW   | INT4_EN  | Enable INT_STATUS[4]  | 0x0           |
| 3     | RW   | INT3_EN  | Enable INT_STATUS[3]  | 0x0           |
| 2     | RW   | INT2_EN  | Enable INT_STATUS[2]  | 0x0           |
| 1     | RW   | INT1_EN  | Enable INT_STATUS[1]  | 0x0           |
| 0     | RW   | INT0_EN  | Enable INT_STATUS[0]  | 0x0           |

FF\_STATUS: FF\_STATUS Register (offset: 0x0010)

| Bits  | Type | Name         | Description                                          | Initial value |
|-------|------|--------------|------------------------------------------------------|---------------|
| 31:16 | -    | -            | Reserved                                             | 0x0           |
| 15:12 | RO   | CH1RFF_AVCNT | CH1, Available FIFO space can be read (unit=word)    | 0x0           |
| 11:8  | RO   | CH1TFF_EPCNT | CH1, Available FIFO space can be written (unit=word) | 0x8           |
| 7:4   | RO   | CH0RFF_AVCNT | CH0, Available FIFO space can be read (unit=word)    | 0x0           |
| 3:0   | RO   | CH0TFF_EPCNT | CH0, Available FIFO space can be written (unit=word) | 0x8           |

CH0\_CFG: CH0\_CFG Register (offset: 0x0020)

| Bits  | Type | Name       | Description                                                                                                                                                                                                                                                                    | Initial value |
|-------|------|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31    | RW   | LBK_EN     | Loopback enable<br>1: loopback<br>(Asyn-TXFIFO→DTX→DRX→Asyn-RXFIFO)<br>0: normal mode                                                                                                                                                                                          | 0x0           |
| 30    | RW   | EXT_LBK_EN | External loopback enable<br>1: external loopback enable<br>(Ext-Codec→DRX→DTX→Ext-Codec)<br>0: normal mode                                                                                                                                                                     | 0x0           |
| 29:27 | RW   | CMP_MODE   | Compress type select<br>000: disable HW converter, linear raw-data (16-bits)<br>010: disable HW converter, linear raw-data(8-bits), A-law or U-law (8-bits)<br>011: reserved<br>100: enable HW converter, raw-data(16-bits) → U-law mode (8-bits) (PCM bus be compress format) | 0x0           |

|       |    |          |                                                                                                                                                                                                                                                                                                        |     |
|-------|----|----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|
|       |    |          | 101: enable HW converter, U-law mode (8-bits) → raw-data(16-bits) (PCM bus be raw-16bits format)<br>110: enable HW converter, raw-data(16-bits) → A-law mode (8-bits) (PCM bus be compress format)<br>111: enable HW converter, A-law mode (8-bits) → raw-data(16-bits) (PCM bus be raw-16bits format) |     |
| 26:10 | -  | -        | Reserved                                                                                                                                                                                                                                                                                               | 0x0 |
| 9:0   | RW | TS_START | Timeslot Starting location                                                                                                                                                                                                                                                                             | 0x1 |

**CH1\_CFG: CH1\_CFG Register (offset: 0x0024)**

| Bits  | Type | Name       | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | Initial value |
|-------|------|------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31    | RW   | LBK_EN     | Loopback enable<br>1: loopback<br>(Asyn-TXFIFO → DTX → DRX → Asyn-RXFIFO)<br>0: normal mode                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | 0x0           |
| 30    | RW   | EXT_LBK_EN | External loopback enable<br>1: external loopback enable<br>(Ext-Codec → DRX → DTX → Ext-Codec)<br>0: normal mode                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | 0x0           |
| 29:27 | RW   | CMP_MODE   | Compress type select<br>000: disable HW converter, linear raw-data (16-bits)<br>010: disable HW converter, linear raw-data(8-bits), A-law or U-law (8-bits)<br>011: reserved<br>100: enable HW converter, raw-data(16-bits) → U-law mode (8-bits) (PCM bus be compress format)<br>101: enable HW converter, U-law mode (8-bits) → raw-data(16-bits) (PCM bus be raw-16bits format)<br>110: enable HW converter, raw-data(16-bits) → A-law mode (8-bits) (PCM bus be compress format)<br>111: enable HW converter, A-law mode (8-bits) → raw-data(16-bits) (PCM bus be raw-16bits format) | 0x0           |
| 26:10 | -    | -          | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | 0x0           |
| 9:0   | RW   | TS_START   | Timeslot Starting location                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | 0x1           |

**FSYNC\_CFG: : FSYNC configuration Register (offset:0x0030)**

| Bits  | Type | Name         | Description                                                                                                                                                | Initial value |
|-------|------|--------------|------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31    | RW   | Cfg_fsycn_en | Enable configurable FSYNC                                                                                                                                  | 0x0           |
| 30    | RW   | Pos_sample   | Controller sample data with<br>1: positive edge of PCM clock<br>0: negative edge of PCM clock<br><br>Notice: This configuration should be "0" if DTX_TRI=1 | 0x0           |
| 29:22 | -    | -            | Reserved                                                                                                                                                   | 0x0           |
| 21:12 | RW   | Fsync_start  | Start point of configurable FSYNC                                                                                                                          | 0x0           |
| 11:10 | -    | -            | Reserved                                                                                                                                                   | 0x0           |
| 9:0   | RW   | Fsync_intv   | Interval of configurable FSYNC                                                                                                                             | 0x0           |

**CH\_CFG2: : Extended channel configuration Register (offset:0x0034)**

| Bits  | Type | Name         | Description                                                | Initial value |
|-------|------|--------------|------------------------------------------------------------|---------------|
| 31:20 | -    | -            | -                                                          | -             |
| 19    | RW   | CH1_RXFF_CLR | CH1 RXFIFO clear, set 1 for clear, 0 for normal operation. | 0x0           |
| 18    | RW   | CH1_TXFF_CLR | CH1 TXFIFO clear, set 1 for clear, 0 for normal operation. | 0x0           |

|      |    |              |                                                            |     |
|------|----|--------------|------------------------------------------------------------|-----|
| 17   | -  | -            | Reserved                                                   | 0x0 |
| 16   | RW | CH1_LSB      | Enable CH1 transmit in LSB order                           | 0x0 |
| 15:4 | -  | -            | Reserved                                                   | 0x0 |
| 3    | RW | CH0_RXFF_CLR | CH0 RXFIFO clear, set 1 for clear, 0 for normal operation. | 0x0 |
| 2    | RW | CH0_TXFF_CLR | CH0 TXFIFO clear, set 1 for clear, 0 for normal operation. | 0x0 |
| 1    | RW | -            | Reserved                                                   | 0x0 |
| 0    | RW | CH0_LSB      | Enable CH0 transmit in LSB order                           | 0x0 |

RSV\_REG16: RSV\_REG16 Register (offset: 0x0038)

| Bits  | Type | Name      | Description               | Initial value |
|-------|------|-----------|---------------------------|---------------|
| 31:16 | -    | -         | Reserved                  | 0x0           |
| 15:0  | RW   | SPARE_REG | Spare Register for future | 0x0           |

DIVCOMP\_Cfg: Integer part of Divisor Register (offset: 0x0050)

| Bits | Type | Name    | Description               | Initial value |
|------|------|---------|---------------------------|---------------|
| 31   | RW   | CLK_EN  | Enable the clock divisor. | 0x0           |
| 30:8 | -    | -       | Reserved                  | 0x0           |
| 7:0  | RW   | DIVCOMP | fraction part of divisor. | 0x0           |

DIVINT\_Cfg: Integer part of Divisor Register (offset: 0x0054)

| Bits  | Type | Name   | Description                                                                                                                                                            | Initial value |
|-------|------|--------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:10 | -    | -      | Reserved                                                                                                                                                               | 0x0           |
| 9:0   | RW   | DIVINT | Integer part of divisor.<br>Formula :<br>$\text{FreqOut} = 1 / (\text{FreqIn} * 2 * (\text{DIVINT} + \text{DIVCOMP} / (2^8)))$<br><br>FreqIn is always fixed to 40MHz. | 0x0           |

DIGDELAY\_Cfg: Digital delay configuration Register (offset: 0x0060)

| Bits  | Type | Name           | Description                                                                                            | Initial value |
|-------|------|----------------|--------------------------------------------------------------------------------------------------------|---------------|
| 31    | RW   | TXD_CLR_GLT    | Clear the detected glitch flag for TXD. 1:clear, 0:nothing                                             | 0x0           |
| 30    | RW   | CHEN_CLR_GLT   | Clear the detected glitch flag for CHEN. 1:clear, 0:nothing                                            | 0x0           |
| 29:27 | -    | -              | Reserved.                                                                                              | 0x0           |
| 26    | RO   | TXD_GLT_ST     | Status if detect glitch in TXD signal. It can be cleared by bit[31]                                    | 0x0           |
| 25:24 | -    | -              | Reserved.                                                                                              | 0x0           |
| 23    | RO   | CHEN1N_GLT_ST  | Status if detect glitch in CHEN-1 signal. It can be cleared by bit[30] (negedge sample)                | 0x0           |
| 22    | RO   | CHEN0N_GLT_ST  | Status if detect glitch in CHEN-1 signal. It can be cleared by bit[30] (negedge sample)                | 0x0           |
| 21:20 | -    | -              | Reserved.                                                                                              | 0x0           |
| 19    | RO   | CHEN1P_GLT_ST  | Status if detect glitch in CHEN-1 signal. It can be cleared by bit[30] (posedge sample)                | 0x0           |
| 18    | RO   | CHEN0P_GLT_ST  | Status if detect glitch in CHEN-1 signal. It can be cleared by bit[30] (posedge sample)                | 0x0           |
| 17    | RO   | CHEN1PD_GLT_ST | Status if detect glitch in CHEN-1 signal. It can be cleared by bit[30] (posedge sample, delay 1 cycle) | 0x0           |
| 16    | RO   | CHEN0PD_GLT_ST | Status if detect glitch in CHEN-1 signal. It can be cleared by bit[30] (posedge sample, delay 1 cycle) | 0x0           |
| 15    | RW   | TXD_DIGDLY_EN  | Enable digital delay path. 1: enable, 0 disable.                                                       | 0x0           |

|       |    |                |                                                                                                                                                                                                                                               |     |
|-------|----|----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|
| 14:13 | -  | -              | Reserved                                                                                                                                                                                                                                      | 0x0 |
| 12:8  | RW | TXD_DLYVAL     | Delay count value,                                                                                                                                                                                                                            | 0x2 |
| 7     | RW | CHEN_DIGDLY_EN | Enable digital delay path. 1: enable, 0 disable.                                                                                                                                                                                              | 0x0 |
| 6:5   | -  | -              | Reserved                                                                                                                                                                                                                                      | 0x0 |
| 4:0   | RW | CHEN_DLYVAL    | Delay count value,<br>the error of delay<br>= clk_period * (sync_delay + sync_delta + (dlycnt_cfg) + 1)<br>e.g. sync_delay=2, dlyval=2<br>final delay = clk_period * (2 + (-1/0/+1) + (2) + 1)<br>= clk_period * (4/5/6) = clk_period * (4~6) | 0x2 |

CH0\_FIFO: CH0\_FIFO Register (offset: 0x0080)

| Bits | Type | Name     | Description       | Initial value |
|------|------|----------|-------------------|---------------|
| 31:0 | RW   | CH0_FIFO | FIFO access point | 0x0           |

CH1\_FIFO: : CH1\_FIFO Register (offset:0x0084)

| Bits | Type | Name     | Description       | Initial value |
|------|------|----------|-------------------|---------------|
| 31:0 | RW   | CH1_FIFO | FIFO access point | 0x0           |

PCM initialization flow:

Step #1: Set PCM\_CFG

Step #2: Set CH0/1\_CFG

Step #3: Write PCM data to FIFO CH0/1\_FIFO

Step #4: Set GLB\_CFG to enable the PCM and channel.

**Step #5: Set divisor clock**

Step #6: enable clock

Step #7: Monitor FF\_STATUS to receive/transmit the other PCM data.

Example of PCM configuration

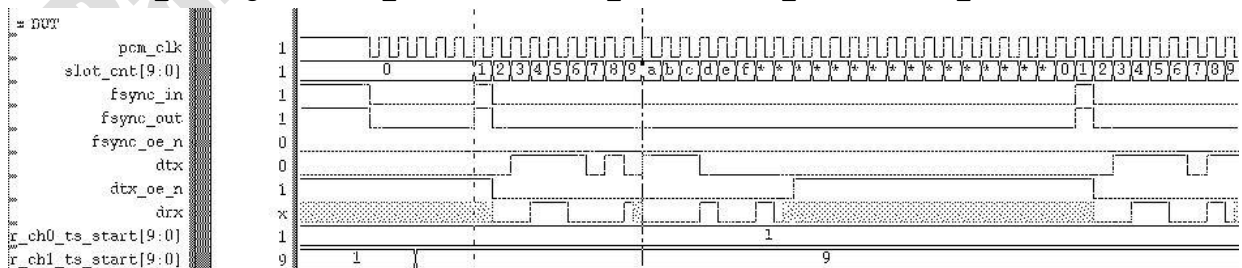
Case1 :

Cfg\_fsycn Register: Cfg\_fsycn\_en = 0 (PS: fsync is always driven at slot\_cnt=1)

CH0\_CFG Register: ts\_start=1

CH1\_CFG Register: ts\_start=9

PCM\_CFG Register: LONG\_FSYNC=1'b0, FSYNC\_POL=1'b1, DRX\_TRI=1'b0, SLOT\_MODE=3'b0



Case2 :

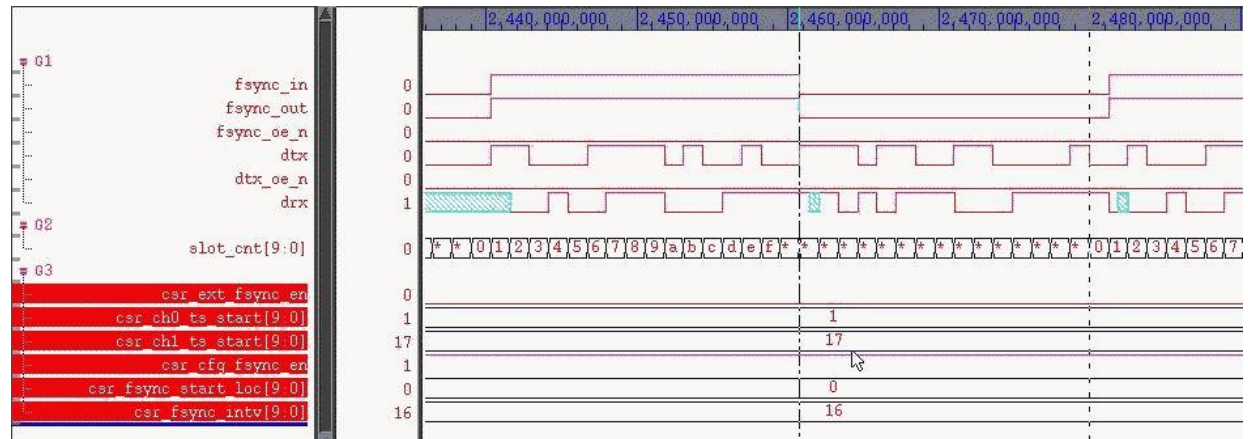
Cfg\_fsyc Register: Cfg\_fsyc\_en = 1, start\_loc=0, interval=16

CH0\_CFG Register: ts\_start=1

CH1\_CFG Register: ts\_start=17

PCM\_CFG Register: LONG\_FSYNC=1'b0, FSYNC\_POL=1'b1, DRX\_TRI=1'b0, SLOT\_MODE=3'b0, RAW16-

bits



Case3 :

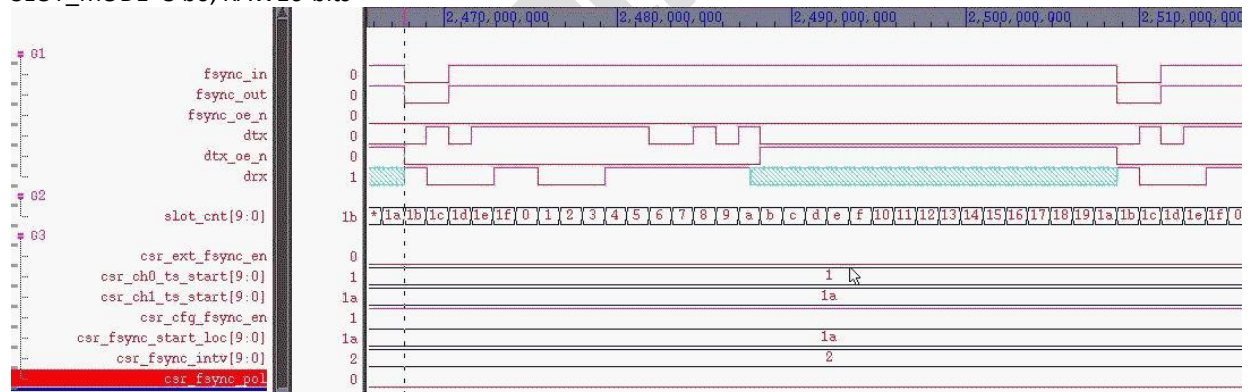
Cfg\_fsyc Register: Cfg\_fsyc\_en = 1, start\_loc=0x1A, interval=2

CH0\_CFG Register: ts\_start=1 (disable)

CH1\_CFG Register: ts\_start=0x1A

PCM\_CFG Register: LONG\_FSYNC=1'b0, FSYNC\_POL=1'b0 (LOW active), DRX\_TRI=1'b0,

SLOT\_MODE=3'b0, RAW16-bits



### 3.13 Generic DMA Controller

#### 3.13.1 Features

- Support 16 DMA channels
- Support 16 DMA requests
- Programmable hardware channel priority
- Programmable DMA Burst Size (1,2,4,8,16 burst transfer)
- Support 32 bit wide transaction
- Big-endian and Little-endian support
- Support memory to memory, memory to peripheral, peripheral to memory, peripheral to peripheral transfers.
- Interrupts for each channel. They also can be masked, independently.
- Each channel transaction can be masked temporarily by the software, and released by the hardware automatically

#### 3.13.2 Block Diagram

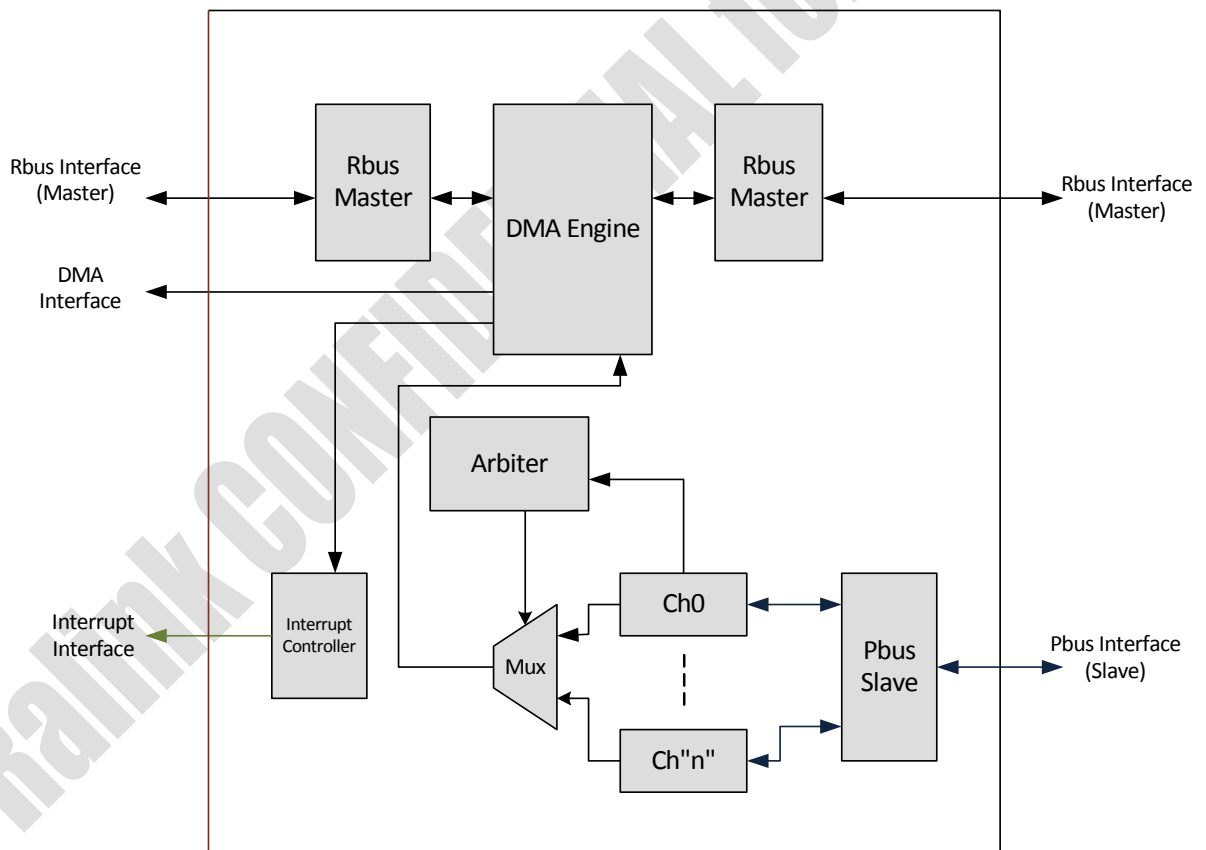


Fig.3-12-1 Generic DMA controller block diagram

#### 3.13.3 Peripheral Channel Connection

| Channel number | Peripheral                       |
|----------------|----------------------------------|
| 0~1            | Reserved                         |
| 2              | I2S Controller (TXDMA)           |
| 3              | I2S Controller (RXDMA)           |
| 4              | PCM Controller (RDMA, channel-0) |
| 5              | PCM Controller (RDMA, channel-1) |
| 6              | PCM Controller (TDMA, channel-0) |
| 7              | PCM Controller (TDMA, channel-1) |
| 8~15           | Reserved                         |

### 3.13.4 Register Description (base: 0x1000\_2800)

GDMA\_SAN: GDMA Channel n Source Address(offset: 0x0000, 0x0010, 0x0020, 0x0030, 0x0040, 0x0050, 0x0060, 0x0070, 0x0080, 0x0090, 0x00a0, 0x00b0, 0x00c0, 0x00d0, 0x00e0, 0x00f0)  
(n:0~15)

| Bits | Type | Name                   | Description                                                                      | Initial value |
|------|------|------------------------|----------------------------------------------------------------------------------|---------------|
| 31:0 | RW   | CHANNEL SOURCE ADDRESS | Channel Source Address:<br>This register contains the source address information | 0x0           |

GDMA\_DAn: GDMA Channel n Destination Address(offset: 0x0004, 0x0014, 0x0024, 0x0034, 0x0044, 0x0054, 0x0064, 0x0074, 0x0084, 0x0094, 0x00a4, 0x00b4, 0x00c4, 0x00d4, 0x00e4, 0x00f4)  
(n:0~15)

| Bits | Type | Name                        | Description                                                                                | Initial value |
|------|------|-----------------------------|--------------------------------------------------------------------------------------------|---------------|
| 31:0 | RW   | CHANNEL DESTINATION ADDRESS | Channel Destination Address:<br>This register contains the destination address information | 0x0           |

GDMA\_CTOn: GDMA Channel n Control Register 0(offset: 0x0008, 0x0018, 0x0028, 0x0038, 0x0048, 0x0058, 0x0068, 0x0078, 0x0088, 0x0098, 0x00a8, 0x00b8, 0x00c8, 0x00d8, 0x00e8, 0x00f8)  
(n:0~15)

| Bits  | Type | Name                   | Description                                                                               | Initial value |
|-------|------|------------------------|-------------------------------------------------------------------------------------------|---------------|
| 31:16 | RW   | Transfer Count         | These registers contain the number of the data bytes needed to be transfer.               | 0x0           |
| 15:8  | -    | -                      | Reserved                                                                                  | 0x0           |
| 7     | RW   | Source Burst Mode      | The value represents the source burst mode<br>'b0: incremental mode<br>'b1: fix mode      | 0x0           |
| 6     | RW   | Destination Burst Mode | The value represents the destination burst mode<br>'b0: incremental mode<br>'b1: fix mode | 0x0           |



|     |    |                                |                                                                                                                                                                                                                                                     |     |
|-----|----|--------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|
| 5:3 | RW | Burst Size                     | The number of the transfer for burst transaction.<br>'b000: 1 transfer<br>'b001: 2 transfer<br>'b010: 4 transfer<br>'b011: 8 transfer<br>'b100: 16 transfer<br>others: undefined                                                                    | 0x0 |
| 2   | RW | Transmit Done Interrupt Enable | Transmit done interrupt enable.<br>'b1: Enable<br>'b0: Disable                                                                                                                                                                                      | 0x0 |
| 1   | RW | Channel Enable                 | Enable the channel<br>'b1: Enable<br>'b0: Disable<br>This bit will be de-asserted by the hardware when the transaction is done.                                                                                                                     | 0x0 |
| 0   | RW | Hardware/Software Mode Select  | Hardware/Software Mode Select<br>'b1: Software Mode<br>'b0: Hardware Mode<br>In software mode, the data transfer will start when the Channel Enable bit is set.<br>In hardware mode, the data transfer will start when the DMA Request is asserted. | 0x0 |

GDMA\_CT1n: GDMA Channel n Control Register 1(offset: 0x000c, 0x001c, 0x002c, 0x003c, 0x004c, 0x005c, 0x006c, 0x007c, 0x008c, 0x009c, 0x00ac, 0x00bc, 0x00cc, 0x00dc, 0x00ec, 0x00fc)

(n:0~15)

| Bits  | Type | Name                    | Description                                                                                                                                                                                              | Initial value |
|-------|------|-------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:22 | -    | -                       | Reserved                                                                                                                                                                                                 | 0x0           |
| 21:16 | RW   | Source DMA Request      | The value represents the source DMA request.<br>0: DMA_REQ0<br>1: DMA_REQ1<br>2: DMA_REQ2<br>...<br>n: DMA_REQn<br>32: The source of the transfer is memory<br>others: undefined                         | 0x0           |
| 15:14 | -    | -                       | Reserved                                                                                                                                                                                                 | 0x0           |
| 13:8  | RW   | Destination DMA Request | The value represents the destination DMA request.<br>0: DMA_REQ0<br>1: DMA_REQ1<br>2: DMA_REQ2<br>...<br>n: DMA_REQn<br>32: The destination of the transfer is memory<br>others: undefined               | 0x0           |
| 7:3   | RW   | Next Unmasked Channel   | The value represents the next unmasked channel. When the transaction is done, the hardware will clear the Channel Mask bit of the next unmasked channel.<br>0: Channel 0<br>1: Channel 1<br>2: Channel 2 | 0x0           |



|   |    |                                   |                                                                                                                                                                                                                                                                   |     |
|---|----|-----------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|
|   |    |                                   | ...<br>n: Channel n<br>If the hardware doesn't need to clear any Channel Mask bit, these bits must be set to their own channel.                                                                                                                                   |     |
| 2 | RW | Coherent Interrupt Enable         | When set to 1'b1, GDMA will issue a dummy READ to Destination after last WRITE to Destination. This can ensure the last WRITE arrived at MEM and avoid race problem between interrupt and data to MEM. (please don't set this to 1'b1 if destination is not MEM). | 0x0 |
| 1 | RW | Channel Unmasked Interrupt Enable | Channel unmasked interrupt enable.<br>'b1: Enable<br>'b0: Disable<br>When this bit is set, an interrupt will be asserted when the hardware wants to clear the Channel Mask bit and the Channel Mask bit is 0 originally.                                          | 0x0 |
| 0 | RW | Channel Mask                      | Channel Mask<br>'b1: This channel is masked<br>'b0: This channel is not masked<br>When this channel mask is set, the GDMA transaction will not start until this bit is clear by the hardware.                                                                     | 0x0 |

**GDMA\_UNMASKINT: GDMA Unmasked Interrupt Status Register (offset: 0x0200)**

| Bits | Type | Name                      | Description                                                                                                                                                                                                                         | Initial value |
|------|------|---------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:0 | W1C  | Unmasked Interrupt Status | This register contains the unmasked interrupt status. This bit will be set when the hardware wants to clear the Channel Mask bit and the Channel Mask bit is 0 originally.<br>Bitn~bit0 is for channel-n ~ channel-0, respectively. | 0x0           |

**GDMA\_DONEINT: GDMA Interrupt Status Register (offset: 0x0204)**

| Bits | Type | Name                           | Description                                                                                                         | Initial value |
|------|------|--------------------------------|---------------------------------------------------------------------------------------------------------------------|---------------|
| 31:0 | W1C  | Transmit Done Interrupt Status | This register contains the transmit-done interrupt status.<br>Bitn~bit0 is for channel-n ~ channel-0, respectively. | 0x0           |

**GDMA\_GCT: GDMA Global Control Register (offset: 0x0220)**

| Bits | Type | Name                  | Description                                                                                                                                                                                                          | Initial value |
|------|------|-----------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:5 | -    | -                     | Reserved                                                                                                                                                                                                             | -             |
| 4:3  | RO   | Total channel number  | 2'b0: 8 channel<br>2'b1: 16 channel<br>2'b2: 32 channel<br>2'b3: Reserved                                                                                                                                            | 0x1           |
| 2:1  | RO   | IP version            | Version of GDMA core                                                                                                                                                                                                 | 0x2           |
| 0    | RW   | Arbitration Selection | Select the channel arbitration method.<br>1'b0: Channel-0 has the highest priority. Channel-1~ Channel-n are round-robin.<br>1'b1: Channel-0 doesn't have the highest priority. Channel-0~Channel-n are round-robin. | 0x0           |

**GDMA\_REQSTS: GDMA Request Status Register (offset: 0x02a0)**

| Bits | Type | Name                       | Description                                                                                                     | Initial value |
|------|------|----------------------------|-----------------------------------------------------------------------------------------------------------------|---------------|
| 31:0 | RO   | GDMA Request Signal Status | This register contains the GDMA Request Signals status<br>Bitn~bit0 is for GDMA_REQn ~ GDMA_REQ0, respectively. | 0x0           |

**GDMA\_ACKSTS: GDMA Acknowledge Status Register (offset: 0x02a4)**

| Bits | Type | Name                           | Description                                                                                                         | Initial value |
|------|------|--------------------------------|---------------------------------------------------------------------------------------------------------------------|---------------|
| 31:0 | RO   | GDMA Acknowledge Signal Status | This register contains the GDMA Acknowledge Signals status<br>Bitn~bit0 is for GDMA_ACKn ~ GDMA_ACK0, respectively. | 0x0           |

**GDMA\_FINSTS: GDMA Finish Status Register (offset: 0x02a8)**

| Bits | Type | Name                      | Description                                                                                                          | Initial value |
|------|------|---------------------------|----------------------------------------------------------------------------------------------------------------------|---------------|
| 31:0 | RO   | GDMA Finish Signal Status | This register contains the GDMA Finish Signals status<br>Bitn~bit0 is for GDMA_FINISHn ~ GDMA_FINISH0, respectively. | 0x0           |

### 3.14 SPI Controller

#### 3.14.1 Features

- Supports up to 2 SPI master operations
- Programmable clock polarity
- Programmable interface clock rate
- Programmable bit ordering
- Firmware-controlled SPI enable
- Programmable payload (address + data) length

#### 3.14.2 Block Diagram

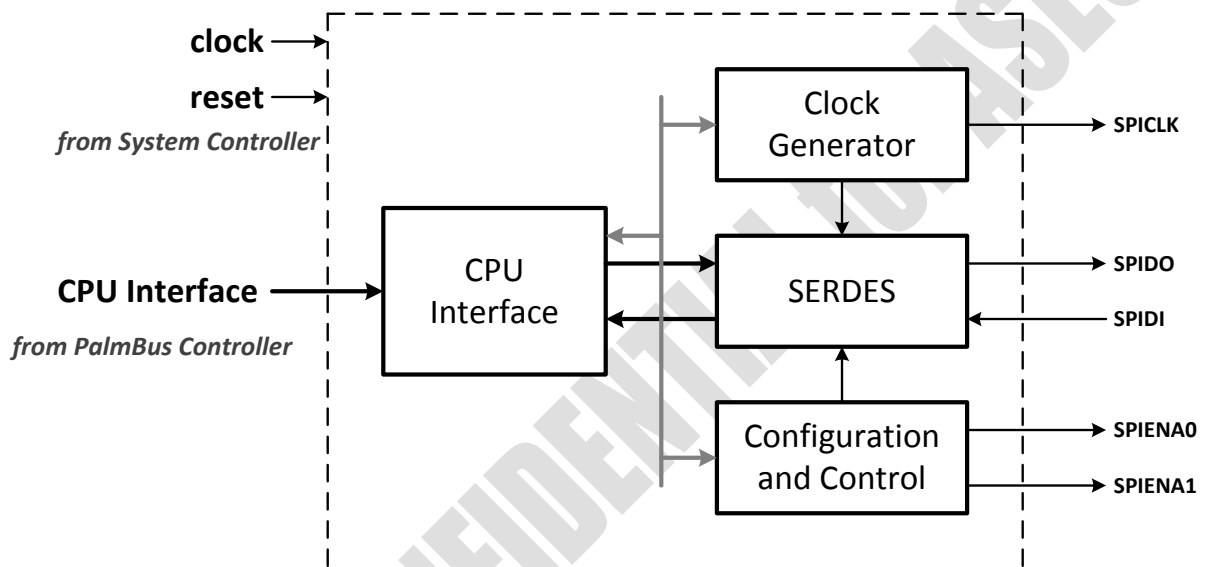


Fig. 3-11-1 SPI controller Block Diagram

#### 3.14.3 Register Description (base: 0x1000\_0b00)

SPISTAT0: SPI Interface 0 Status (offset: 0x0000)

| Bits | Type | Name | Description                                                                                                                                                                                                                                | Initial value |
|------|------|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:1 | -    | -    | Reserved                                                                                                                                                                                                                                   | 0x0           |
| 0    | RO   | BUSY | SPI transfer in progress<br>0: The SPI interface is inactive.<br>1: An SPI transfer is in progress.<br>Note: This bit must be '0' before initiating a transfer. Any attempt to start a data transfer will be ignored if this bit is a '1'. | 0x0           |

SPICFG0: SPI Interface 0 Configuration (offset: 0x0010)

| Bits | Type | Name     | Description                                                                                                                                                        | Initial value |
|------|------|----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:9 | -    | -        | Reserved                                                                                                                                                           | 0x0           |
| 8    | RW   | MSBFIRST | Bit transfer order<br>0: LSB bits of data sent/received first.<br>1: MSB bits of data sent/received first.<br>Note: This bit applies to both the command and data. | 0x1           |
| 7    | -    | -        | Reserved                                                                                                                                                           | 0x0           |

|     |    |             |                                                                                                                                                                                                                                                                                                                                                                                                                                     |     |
|-----|----|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|
| 6   | RW | SPICLKPOL   | SPI clock default state<br>0: The default state of the SPICLK is logic '0'.<br>1: The default state of the SPICLK is logic '1'.<br>Note: This bit is ignored if the SPI interface block is a slave (SPISLAVE bit is set).                                                                                                                                                                                                           | 0x0 |
| 5   | RW | RXCKEDGE    | SPI clock default state<br>0: Data is captured on the rising edge of the SPICLK signal.<br>1: Data is captured on the falling edge of the SPICLK signal.                                                                                                                                                                                                                                                                            | 0x0 |
| 4   | RW | TXCKEDGE    | SPI clock default state<br>0: Data is transmitted on the rising edge of the SPICLK signal.<br>1: Data is transmitted on the falling edge of the SPICLK signal.                                                                                                                                                                                                                                                                      | 0x0 |
| 3   | RW | HIZSPI      | Tri-state all SPI pin<br>0: SPICLK and SPIENA pin are driven.<br>1: SPICLK and SPIENA pin are tri-stated.<br>Note: This bit overrides all normal functionality.                                                                                                                                                                                                                                                                     | 0x0 |
| 2:0 | RW | SPICLK[2:0] | SPI clock divide control<br>(the rate in following table should be change in the future)<br>0: SPICLK rate is system clock rate / 2<br>1: SPICLK rate is system clock rate / 4<br>2: SPICLK rate is system clock rate / 8<br>3: SPICLK rate is system clock rate / 16<br>4: SPICLK rate is system clock rate / 32<br>5: SPICLK rate is system clock rate / 64<br>6: SPICLK rate is system clock rate / 128<br>7: SPICLK is disabled | 0x0 |

**SPICTL0: SPI Interface 0 Control (offset: 0x0014)**

| Bits | Type | Name    | Description                                                                                                                                                                                                                                                                                                                                                                                                 | Initial value |
|------|------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:4 | -    | -       | Reserved                                                                                                                                                                                                                                                                                                                                                                                                    | 0x0           |
| 3    | RW   | HIZSDO  | Tri-state data out<br>0: The SPIDO pin remains driven after the cycle is complete.<br>1: The SPIDO pin is tri-stated after the cycle is complete.<br>Note: This bit applies to write transfers only; for read transfers the SPIDO pin is tri-stated during the transfer.                                                                                                                                    | 0x0           |
| 2    | RW   | STARTWR | Start SPI write transfer<br>When this bit is written with a '1', the contents of the SPIDATA register are transferred to the SPI slave device. Writing a '0' to this register has no effect.<br>Note: The BUSY bit in the SPISTAT register is set when this bit is set and is cleared when the data transfer is complete. This bit is only meaningful if the SPI interface block is configured as a master. | 0x0           |
| 1    | RW   | STARTRD | When this bit is written with a '1', a read from the SPI slave is started; the read data is placed in the SPIDATA register. Writing a '0' to this register has no effect.<br>Note: The BUSY bit in the SPISTAT register is set when a this bit is set and is cleared when the data transfer is complete. This bit is only meaningful if the SPI interface block is configured as a master.                  | 0x0           |
| 0    | RW   | SPIENA  | 0: The SPIENA pin is negated.<br>1: The SPIENA pin is asserted.                                                                                                                                                                                                                                                                                                                                             | 0x0           |

**SPIDATA0: SPI Interface 0 Data (offset: 0x0020)**

| Bits | Type | Name | Description | Initial value |
|------|------|------|-------------|---------------|
| 31:8 | -    | -    | Reserved    | 0x0           |

|     |    |              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |     |
|-----|----|--------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|
| 7:0 | RW | SPIDATA[7:0] | <p>This register is used for command/data transfers on the SPI interface. The use of this register is given below:</p> <p>Write: the bits to be transferred are written here, including both command and data bits. If values are transmitted MSB (most significant bit) first, the command is placed in the upper bits and the data in the lower bits. Bit 0 of the data is written to SPIDATA [0]; bit 0 of the command follows the MSB of the data. If data is transmitted LSB (least significant bit) first, the command is placed in the lower bits and the data is placed in the upper bits.</p> <p>Read: the command bits are written here. Bit 0 of the command is written to SPIDATA[0]. When the transfer is complete, the data transferred from the slave may be read from the lower bits of this register.</p> | 0x0 |
|-----|----|--------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|

**SPICSTAT1: SPI Interface 1 Status (offset: 0x0040)**

| Bits | Type | Name | Description                                                                                                                                                                                                                                                   | Initial value |
|------|------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:2 | -    | -    | Reserved                                                                                                                                                                                                                                                      | 0x0           |
| 0    | RO   | BUSY | <p>SPI transfer in progress</p> <p>0: The SPI interface is inactive.</p> <p>1: An SPI transfer is in progress.</p> <p>Note: This bit must be '0' before initiating a transfer. Any attempt to start a data transfer will be ignored if this bit is a '1'.</p> | 0x0           |

**SPICFG1: SPI Interface 1 Configuration (offset: 0x0050)**

| Bits | Type | Name      | Description                                                                                                                                                                                                                                  | Initial value |
|------|------|-----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:9 | -    | -         | Reserved                                                                                                                                                                                                                                     | 0x0           |
| 8    | RW   | MSBFIRST  | <p>Bit transfer order</p> <p>0: LSB bits of data sent/received first.</p> <p>1: MSB bits of data sent/received first.</p> <p>Note: This bit applies to both the command and data.</p>                                                        | 0x1           |
| 7    | -    | -         | Reserved                                                                                                                                                                                                                                     | 0x0           |
| 6    | RW   | SPICLKPOL | <p>SPI clock default state</p> <p>0: The default state of the SPICLK is logic '0'.</p> <p>1: The default state of the SPICLK is logic '1'.</p> <p>Note: This bit is ignored if the SPI interface block is a slave (SPISLAVE bit is set).</p> | 0x0           |
| 5    | RW   | RXCKEDGE  | <p>SPI clock default state</p> <p>0: Data is captured on the rising edge of the SPICLK signal.</p> <p>1: Data is captured on the falling edge of the SPICLK signal.</p>                                                                      | 0x0           |
| 4    | RW   | TXCKEDGE  | <p>SPI clock default state</p> <p>0: Data is transmitted on the rising edge of the SPICLK signal.</p> <p>1: Data is transmitted on the falling edge of the SPICLK signal.</p>                                                                | 0x0           |
| 3    | RW   | HIZSPI    | <p>Tri-state all SPI pin</p> <p>0: SPICLK and SPIENA pin are driven.</p> <p>1: SPICLK and SPIENA pin are tri-stated.</p> <p>Note: This bit overrides all normal functionality.</p>                                                           | 0x0           |

|     |    |             |                                                                                                                                                                                                                                                                                                                                                                                                                                     |     |
|-----|----|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|
| 2:0 | RW | SPICLK[2:0] | SPI clock divide control<br>(the rate in following table should be change in the future)<br>0: SPICLK rate is system clock rate / 2<br>1: SPICLK rate is system clock rate / 4<br>2: SPICLK rate is system clock rate / 8<br>3: SPICLK rate is system clock rate / 16<br>4: SPICLK rate is system clock rate / 32<br>5: SPICLK rate is system clock rate / 64<br>6: SPICLK rate is system clock rate / 128<br>7: SPICLK is disabled | 0x0 |
|-----|----|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|

**SPICTL1: SPI Interface 1 Control (offset: 0x0054)**

| Bits | Type | Name    | Description                                                                                                                                                                                                                                                                                                                                                                                                 | Initial value |
|------|------|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:4 | -    | -       | Reserved                                                                                                                                                                                                                                                                                                                                                                                                    | 0x0           |
| 3    | RW   | HIZSDO  | Tri-state data out<br>0: The SPIDO pin remains driven after the cycle is complete.<br>1: The SPIDO pin is tri-stated after the cycle is complete.<br>Note: This bit applies to write transfers only; for read transfers the SPIDO pin is tri-stated during the transfer.                                                                                                                                    | 0x0           |
| 2    | RW   | STARTWR | Start SPI write transfer<br>When this bit is written with a '1', the contents of the SPIDATA register are transferred to the SPI slave device. Writing a '0' to this register has no effect.<br>Note: The BUSY bit in the SPISTAT register is set when this bit is set and is cleared when the data transfer is complete. This bit is only meaningful if the SPI interface block is configured as a master. | 0x0           |
| 1    | RW   | STARTRD | When this bit is written with a '1', a read from the SPI slave is started; the read data is placed in the SPIDATA register. Writing a '0' to this register has no effect.<br>Note: The BUSY bit in the SPISTAT register is set when a this bit is set and is cleared when the data transfer is complete. This bit is only meaningful if the SPI interface block is configured as a master.                  | 0x0           |
| 0    | RW   | SPIENA  | 0: The SPIENA pin is negated.<br>1: The SPIENA pin is asserted.                                                                                                                                                                                                                                                                                                                                             | 0x0           |

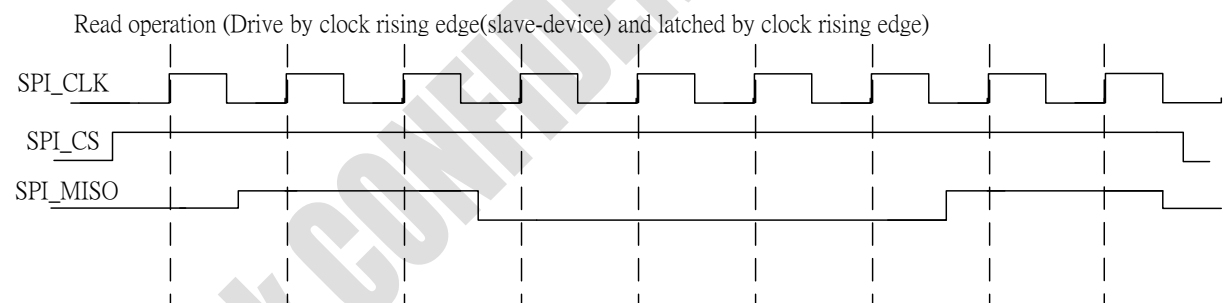
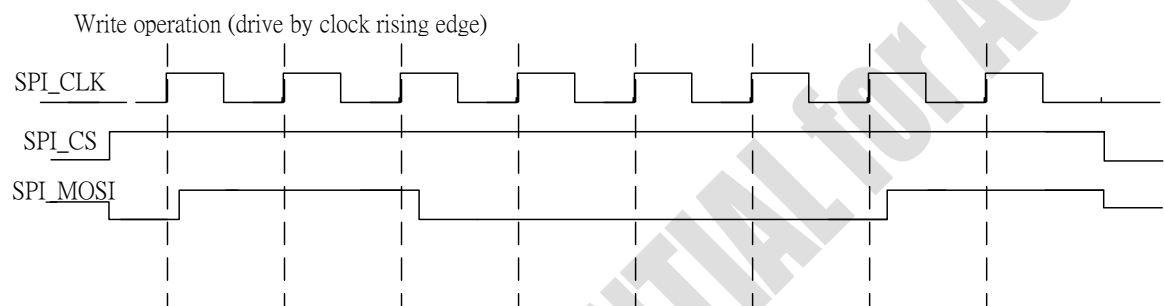
**SPIDATA1: SPI Interface 1 Data (offset: 0x0060)**

| Bits | Type | Name         | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | Initial value |
|------|------|--------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:8 | -    | -            | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | 0x0           |
| 7:0  | RW   | SPIDATA[7:0] | This register is used for command/data transfers on the SPI interface. The use of this register is given below:<br>Write: the bits to be transferred are written here, including both command and data bits. If values are transmitted MSB (most significant bit) first, the command is placed in the upper bits and the data in the lower bits. Bit 0 of the data is written to SPIDATA[0]; bit 0 of the command follows the MSB of the data. If data is transmitted LSB (least significant bit) first, the command is placed in the lower bits and the data is placed in the upper bits.<br>Read: the command bits are written here. Bit 0 of the command is written to SPIDATA[0]. When the transfer is complete, the data transferred from the slave may be read from the lower bits of this register. | 0x0           |

**SPIARB: SPI Interface ARBITER (offset: 0x00f0)** (Note: **This register must be configured when SPI interface 1 want to be activated**)

| Bits | Type | Name     | Description                                                                                                                                       | Initial value |
|------|------|----------|---------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31   | RW   | ARB_EN   | Arbiter Enable<br>0: Only SPI interface 0 will work.<br>1: SPI Interface 0/1 will work concurrently.                                              | 0x0           |
| 30:2 | -    | -        | Reserved                                                                                                                                          | 0x0           |
| 1    | RW   | SPI1_POR | The chip enable polarity indicator for SPI interface 1<br>0: Indicate the chip enable is low active<br>1: Indicate the chip enable is high active | 0x1           |
| 0    | RW   | SPI0_POR | The chip enable polarity indicator for SPI interface 0<br>0: Indicate the chip enable is low active<br>1: Indicate the chip enable is high active | 0x1           |

#### Waveform of SPI interface



NOTICE: 1) SPI\_CLK is gated clock.  
2) SPI\_CS is controller by software





### 3.15 I2S Controller

#### 3.15.1 Features

- I<sup>2</sup>S transmitter/Receiver, which can be configured as master or slave.
- Support 16-bit data, sample rate 8Khz, 16Khz, 22.05Khz, 44.1Khz, and 48Khz
- Support stereo audio data transfer.
- 32 bytes FIFO are available for data transmission.
- Support GDMA access
- Support 12Mhz bit clock from external (as slave mode)

#### 3.15.2 Block Diagram

The block diagram of I<sup>2</sup>S Transmitter is shown as below.

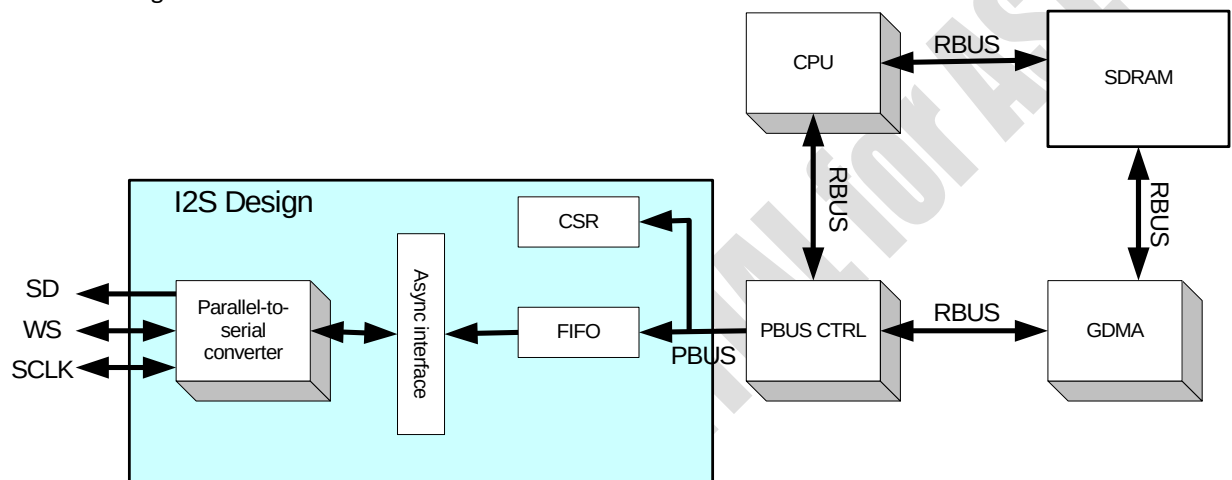


Fig. 5-14-1 The block diagram of I<sup>2</sup>S Transmitter

The I2S interface consists of two separate cores, a transmitter and a receiver. Both can operate in either master or slave mode. Here we will design only the transmitter in master or slave mode.

I<sup>2</sup>S signal timing for I<sup>2</sup>S data format:

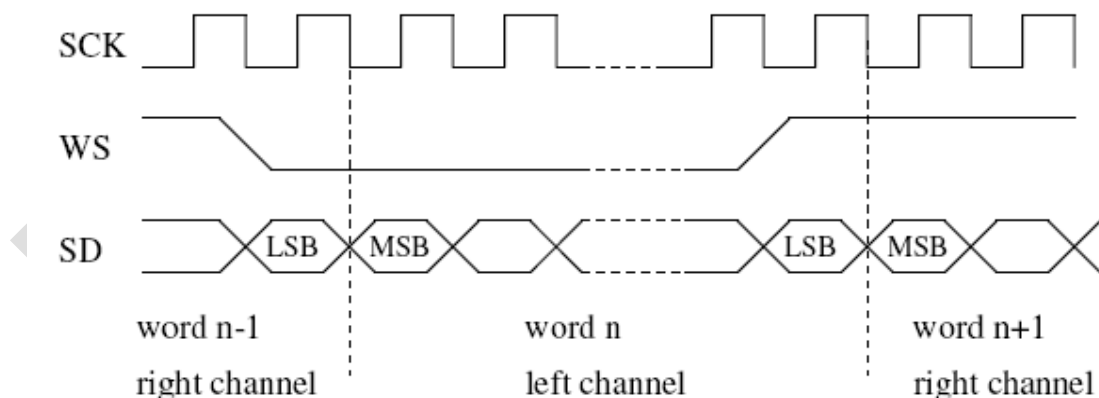


Fig. 5-14-2 I<sup>2</sup>S Transmitter/Receiver

Serial data is transmitted in 2's complement with the MSB first. The transmitter always sends the MSB of the next word one clock period after the WS changes. Serial data sent by the transmitter may be synchronized with either the trailing (HIGH-to-LOW) or the leading (LOW-to-HIGH) edge of the clock signal. However, the serial data must

be latched into the receiver on the leading edge of the serial clock signal, and so there are some restrictions when transmitting data that is synchronized with the leading edge.

The word select line indicates the channel being transmitted:

- WS = 0; channel 1 (left);
- WS = 1; channel 2 (right).

WS may change either on a trailing or leading edge of the serial clock, but it doesn't need to be symmetrical. In the slave, this signal is latched on the leading edge of the clock signal. The WS line changes one clock period before the MSB is transmitted. This allows the slave transmitter to derive synchronous timing of the serial data that will be set up for transmission. Furthermore, it enables the receiver to store the previous word and clear the input for the next Word.

### 3.15.3 Register Description of I2S (base: 0x1000\_0a00)

I2S\_CFG: Tx/Rx Configuration (offset: 0x0000)

| Bits  | Type | Name        | Description                                                                                                    | Initial value |
|-------|------|-------------|----------------------------------------------------------------------------------------------------------------|---------------|
| 31    | RW   | I2S_EN      | I2S enable,<br>1: enable<br>0: disable, all control registers of I2S will be clear to default value.           | 0x0           |
| 30    | RW   | DMA_EN      | DMA Enable<br>1: enable dma access<br>0: disable dma access                                                    | 0x0           |
| 29:25 | -    | Reserved    | Reserved                                                                                                       | 0x0           |
| 24    | RW   | TX_EN       | Transmitter on/off control<br>1: Enable transmitter<br>0: Disable transmitter                                  | 0x0           |
| 23:21 | -    | Reserved    | Reserved                                                                                                       | 0x0           |
| 20    | RW   | RX_EN       | Receiver on/off control<br>1: Enable receiver<br>0: Disable receiver                                           | 0x0           |
| 19:17 | -    | Reserved    | Reserved                                                                                                       | 0x0           |
| 16    | RW   | SLAVE_MODE  | Master os Slave<br>0: Master: using internal clock<br>1: Slave: using external clock                           | 0x1           |
| 15    | -    | Reserved    | Reserved                                                                                                       | 0x0           |
| 14:12 | RW   | RX_FF_THRES | FIFO threshold, As threshold reach, host/dma will notify to fill FIFO. (Unit = word)<br>It should be >2 and <6 | 0x4           |
| 11    | -    | Reserved    | Reserved                                                                                                       | 0x0           |
| 10    | -    | Reserved    | Reserved                                                                                                       | 0x0           |
| 9     | -    | Reserved    | Reserved                                                                                                       | 0x0           |
| 8:7   | -    | Reserved    | Reserved                                                                                                       | 0x0           |
| 6:4   | RW   | TX_FF_THRES | FIFO threshold, As threshold reach, host/dma will notify to fill FIFO. (Unit = word)<br>It should be >2 and <6 | 0x4           |
| 3     | -    | Reserved    | Reserved                                                                                                       | 0x0           |
| 2     | -    | Reserved    | Reserved                                                                                                       | 0x0           |
| 1     | -    | Reserved    | Reserved                                                                                                       | 0x0           |

|   |   |          |          |     |
|---|---|----------|----------|-----|
| 0 | - | Reserved | Reserved | 0x0 |
|---|---|----------|----------|-----|

**INT\_STATUS: I2S Interrupt Status (offset: 0x0004)**

| Bits | Type | Name         | Description                                                           | Initial value |
|------|------|--------------|-----------------------------------------------------------------------|---------------|
| 31:8 | -    | Reserved     | Reserved                                                              | 0x0           |
| 7    | RW   | RX_DMA_FAULT | Find any fault in RX's DMA signals                                    | 0x0           |
| 6    | RW   | RX_OVRUN     | The RX FIFO is overflow (Write '1' to clear)                          | 0x0           |
| 5    | RW   | RX_UNRUN     | The RX FIFO is underflow (Write '1' to clear)                         | 0x0           |
| 4    | RW   | RX_THRES     | The RX FIFO is lower than the defined threshold. (Write '1' to clear) | 0x0           |
| 3    | RW   | TX_DMA_FAULT | Find any fault in TX's DMA signals                                    | 0x0           |
| 2    | RW   | TX_OVRUN     | The TX FIFO is overflow (Write '1' to clear)                          | 0x0           |
| 1    | RW   | TX_UNRUN     | The TX FIFO is underflow (Write '1' to clear)                         | 0x0           |
| 0    | RW   | TX_THRES     | The FIFO is lower than the defined threshold. (Write '1' to clear)    | 0x0           |

**INT\_EN: I2S Interrupt Enable Control Register (offset: 0x0008)**

| Bits | Type | Name       | Description          | Initial value |
|------|------|------------|----------------------|---------------|
| 31:9 | -    | Reserved   | Reserved             | 0x0           |
| 7    | RW   | RX_INT3_EN | Enable INT_STATUS[7] | 0x0           |
| 6    | RW   | RX_INT2_EN | Enable INT_STATUS[6] | 0x0           |
| 5    | RW   | RX_INT1_EN | Enable INT_STATUS[5] | 0x0           |
| 4    | RW   | RX_INT0_EN | Enable INT_STATUS[4] | 0x0           |
| 3    | RW   | TX_INT3_EN | Enable INT_STATUS[3] | 0x0           |
| 2    | RW   | TX_INT2_EN | Enable INT_STATUS[2] | 0x0           |
| 1    | RW   | TX_INT1_EN | Enable INT_STATUS[1] | 0x0           |
| 0    | RW   | TX_INT0_EN | Enable INT_STATUS[0] | 0x0           |

**FF\_STATUS: I2S Tx/Rx FIFO Status (offset: 0x000c)**

| Bits | Type | Name     | Description                         | Initial value |
|------|------|----------|-------------------------------------|---------------|
| 31:8 | -    | Reserved | Reserved                            | 0x0           |
| 7:4  | RO   | RX_AVCNT | Available FIFO space can be read    | 0x0           |
| 3:0  | RO   | TX_EPCNT | Available FIFO space can be written | 0x8           |

**TX\_FIFO\_WREG: Write Data Buffer(offset: 0x0010)**

| Bits | Type | Name          | Description       | Initial value |
|------|------|---------------|-------------------|---------------|
| 31:0 | RW   | TX_FIFO_WDATA | Write data buffer | 0x0           |

**RX\_FIFO\_RREG: Read Data Buffer(offset: 0x0014)**

| Bits | Type | Name          | Description      | Initial value |
|------|------|---------------|------------------|---------------|
| 31:0 | RO   | RX_FIFO_WDATA | Read data buffer | 0x0           |

**I2S\_CFG1: I2S Loopback Test Control Register (offset: 0x0018)**

| Bits | Type | Name       | Description                                                                                                          | Initial value |
|------|------|------------|----------------------------------------------------------------------------------------------------------------------|---------------|
| 31   | RW   | LBK_EN     | Loop Back Enable<br>0: normal mode<br>1: loop back mode<br>Async_txFifio → Tx → Rx → Async_rxFifio                   | 0x0           |
| 30   | RW   | EXT_LBK_EN | External Loop Back Enable<br>0: normal mode<br>1: external loop back enable<br>External A/D → Rx → Tx → External D/A | 0x0           |
| 29:2 | -    | Reserved   | Reserved                                                                                                             | 0x0           |
| 1:0  | -    | Reserved   | Reserved                                                                                                             | 0x0           |

**DIVCOMP\_CFG: Integer part of Divisor Register (offset: 0x0020)**

| Bits | Type | Name    | Description               | Initial value |
|------|------|---------|---------------------------|---------------|
| 31   | RW   | CLK_EN  | Enable the clock divisor. | 0x0           |
| 30:9 | -    | -       | Reserved                  | 0x0           |
| 8:0  | RW   | DIVCOMP | fraction part of divisor. | 0x0           |

**DIVINT\_CFG: Integer part of Divisor Register (offset: 0x0024)**

| Bits  | Type | Name   | Description                                                                                                                                                              | Initial value |
|-------|------|--------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:10 | -    | -      | Reserved                                                                                                                                                                 | 0x0           |
| 9:0   | RW   | DIVINT | Integer part of divisor.<br>Formula :<br>$\text{FreqOut} = \text{FreqIn} * (1/2) * \{1 / [\text{DIVINT} + \text{DIVCOMP} / (512)]\}$<br>FreqIn is always fixed to 40MHz. | 0x0           |

### 3.16 Memory Controller

#### 3.16.1 Features

- Support 2 SDRAM(16b) chip select
- Support 1 SRAM (8/16b) chip selects
- Support 32MB/SDRAM per chip select
- Support SDRAM transaction overlapping by early active and hidden pre-charge
- Support user SDRAM Init commands
- Support 4 banks per SDRAM chip select
- SDRAM burst length: 4 (fixed)
- Support Wrap-4 transfer
- Support Bank-Row-Column and Row-Bank-Column address mapping
- 

#### 3.16.2 Block Diagram

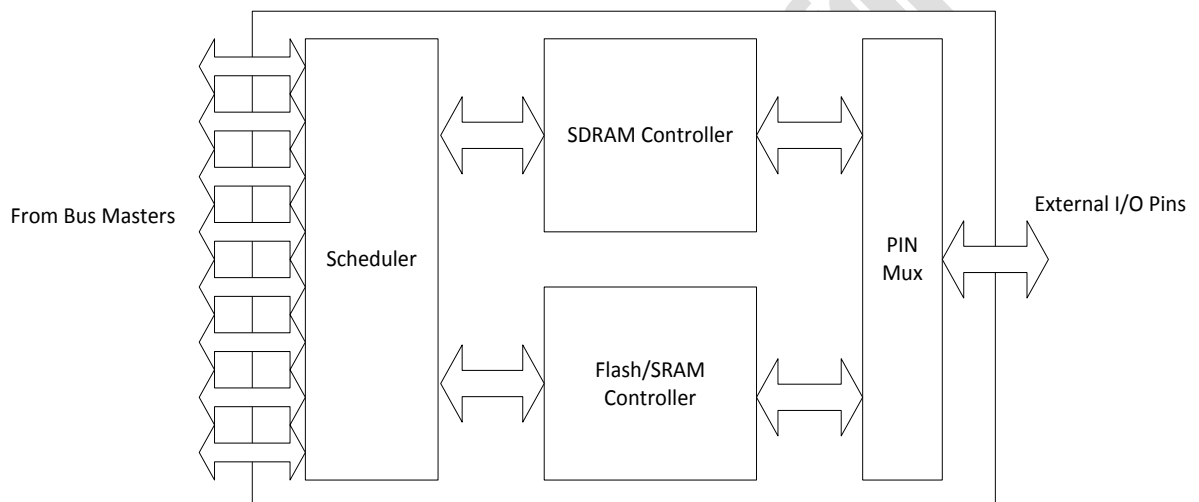


Fig. 3-15-1 SRAM/SDRAM controller Block Diagram

##### 3.16.2.1 SDRAM Initialization Sequence

SDRAMs require an initialization sequence before they are ready for reading and writing. The initialization sequence is described below.

Step #1: setting SDRAM related timing in SDRAM\_CFG0

Step#2: setting SDRAM size and refresh time in SDRAM\_CFG1 register with  
SDRAM\_INIT\_START = 1

Step#3: Read SDRAM\_INIT\_DONE in SDRAM\_CFG1 register

Step#4: if SDRAM\_INIT\_DONE !=1, go to Step#3, else SDRAM initialization sequence finished

Turn off power saving

| Size | DRAM width (16bit),<br>total bus width 16 | DRAM width (16bit),<br>total bus width 32 | DRAM width (32bit),<br>total bus width 32 |
|------|-------------------------------------------|-------------------------------------------|-------------------------------------------|
| 16Mb | SDRAM0: 0xD1825272,<br>SDRAM1: 0xA0000600 | SDRAM0: 0xD1825272,<br>SDRAM1: 0xA1000600 | N/A                                       |
| 64Mb | SDRAM0: 0xD1825272,                       | SDRAM0: 0xD1825272,                       | SDRAM0: 0xD1825272,                       |

|               |                                           |                                           |                                           |
|---------------|-------------------------------------------|-------------------------------------------|-------------------------------------------|
|               | SDRAM1: 0xA0010600                        | SDRAM1: 0xA1010600                        | SDRAM1: 0xA1000600                        |
| <b>128Mb</b>  | SDRAM0: 0xD1825272,<br>SDRAM1: 0xA0110600 | SDRAM0: 0xD1825272,<br>SDRAM1: 0xA1110600 | SDRAM0: 0xD1825272,<br>SDRAM1: 0xA1010600 |
| <b>256Mb</b>  | SDRAM0: 0xD1825272,<br>SDRAM1: 0xA0120600 | SDRAM0: 0xD1825272,<br>SDRAM1: 0xA1120600 | SDRAM0: 0xD1825272,<br>SDRAM1: 0xA1110600 |
| <b>512Mb</b>  | SDRAM0: 0xD1825272,<br>SDRAM1: 0xA0220600 | SDRAM0: 0xD1825272,<br>SDRAM1: 0xA1220600 | SDRAM0: 0xD1825272,<br>SDRAM1: 0xA1120600 |
| <b>1024Mb</b> | N/A                                       | N/A                                       | N/A                                       |
| <b>2048Mb</b> | N/A                                       | N/A                                       | N/A                                       |

**Turn on power saving with precharge power down mode**

| Size          | DRAM width (16bit),<br>total bus width 16 | DRAM width (16bit),<br>total bus width 32 | DRAM width (32bit),<br>total bus width 32 |
|---------------|-------------------------------------------|-------------------------------------------|-------------------------------------------|
| <b>16Mb</b>   | SDRAM0: 0xD1825272,<br>SDRAM1: 0xB0000600 | SDRAM0: 0xD1825272,<br>SDRAM1: 0xB1000600 | N/A                                       |
| <b>64Mb</b>   | SDRAM0: 0xD1825272,<br>SDRAM1: 0xB0010600 | SDRAM0: 0xD1825272,<br>SDRAM1: 0xB1010600 | SDRAM0: 0xD1825272,<br>SDRAM1: 0xB1000600 |
| <b>128Mb</b>  | SDRAM0: 0xD1825272,<br>SDRAM1: 0xB0110600 | SDRAM0: 0xD1825272,<br>SDRAM1: 0xB1110600 | SDRAM0: 0xD1825272,<br>SDRAM1: 0xB1010600 |
| <b>256Mb</b>  | SDRAM0: 0xD1825272,<br>SDRAM1: 0xB0120600 | SDRAM0: 0xD1825272,<br>SDRAM1: 0xB1120600 | SDRAM0: 0xD1825272,<br>SDRAM1: 0xB1110600 |
| <b>512Mb</b>  | SDRAM0: 0xD1825272,<br>SDRAM1: 0xB0220600 | SDRAM0: 0xD1825272,<br>SDRAM1: 0xB1220600 | SDRAM0: 0xD1825272,<br>SDRAM1: 0xB1120600 |
| <b>1024Mb</b> | N/A                                       | N/A                                       | N/A                                       |
| <b>2048Mb</b> | N/A                                       | N/A                                       | N/A                                       |

**Turn on power saving with active power down mode**

| Size          | DRAM width (16bit),<br>total bus width 16 | DRAM width (16bit),<br>total bus width 32 | DRAM width (32bit),<br>total bus width 32 |
|---------------|-------------------------------------------|-------------------------------------------|-------------------------------------------|
| <b>16Mb</b>   | SDRAM0: 0xD1825272,<br>SDRAM1: 0xB8000600 | SDRAM0: 0xD1825272,<br>SDRAM1: 0xB9000600 | N/A (ISSI have no this size)              |
| <b>64Mb</b>   | SDRAM0: 0xD1825272,<br>SDRAM1: 0xB8010600 | SDRAM0: 0xD1825272,<br>SDRAM1: 0xB9010600 | SDRAM0: 0xD1825272,<br>SDRAM1: 0xB9000600 |
| <b>128Mb</b>  | SDRAM0: 0xD1825272,<br>SDRAM1: 0xB8110600 | SDRAM0: 0xD1825272,<br>SDRAM1: 0xB9110600 | SDRAM0: 0xD1825272,<br>SDRAM1: 0xB9010600 |
| <b>256Mb</b>  | SDRAM0: 0xD1825272,<br>SDRAM1: 0xB8120600 | SDRAM0: 0xD1825272,<br>SDRAM1: 0xB9120600 | SDRAM0: 0xD1825272,<br>SDRAM1: 0xB9110600 |
| <b>512Mb</b>  | SDRAM0: 0xD1825272,<br>SDRAM1: 0xB8220600 | SDRAM0: 0xD1825272,<br>SDRAM1: 0xB9220600 | SDRAM0: 0xD1825272,<br>SDRAM1: 0xB9120600 |
| <b>1024Mb</b> | N/A                                       | N/A                                       | N/A                                       |
| <b>2048Mb</b> | N/A                                       | N/A                                       | N/A                                       |

**3.16.3 Register Description (base: 0x1000\_0300)**

SDRAM\_CFG0: SDRAM Configuration 0 (offset: 0x0000)

| Bits  | Type | Name       | Description                                            | Initial value |
|-------|------|------------|--------------------------------------------------------|---------------|
| 31    | RO   | ALWAYS_ONE | Use as an identification for Rbus controller           | 0x1           |
| 30:29 | -    | -          | Reserved                                               | 0x0           |
| 28    | RW   | TWR        | Write Recovery time number of system clock cycles – 1. | 0x1           |

|       |    |      |                                                                                      |     |
|-------|----|------|--------------------------------------------------------------------------------------|-----|
| 27:24 | RW | TMRD | LOAD MODE to any other command delay number of system clock cycles – 1.              | 0x1 |
| 23:20 | RW | TRFC | AUTO REFRESH period number of system clock cycles – 1.                               | 0x9 |
| 19:18 | -  | -    | Reserved                                                                             | 0x0 |
| 17:16 | RW | TCAS | READ command to data valid delay (CAS latency) in number of system clock cycles – 1. | 0x2 |
| 15:12 | RW | TRAS | ACTIVE to PRECHARGE command delay in number of system clock cycles – 1.              | 0x5 |
| 11:10 | -  | -    | Reserved                                                                             | 0x0 |
| 9:8   | RW | TRCD | ACTIVE to READ or WRITE delay in number of system clock cycles – 1.                  | 0x2 |
| 7:4   | RW | TRC  | ACTIVE to ACTIVE command period in number of system clock cycles -1                  | 0x8 |
| 3:2   | -  | -    | Reserved                                                                             | 0x0 |
| 1:0   | RW | TRP  | PRECHARGE command period in number of system clock cycles –1.                        | 0x2 |

**SDRAM\_CFG1: SDRAM Configuration 1 (offset: 0x0004)**

| Bits  | Type | Name             | Description                                                                                                                                                                                          | Initial value |
|-------|------|------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31    | RW   | SDRAM_INIT_START | Write 1 to perform SDRAM initialization sequence. Can not set it to zero after initialization.                                                                                                       | 0x0           |
| 30    | RO   | SDRAM_INIT_DONE  | 0: SDRAM has not been initialized<br>1: SDRMA has been initialized                                                                                                                                   | 0x0           |
| 29    | RW   | RBC_MAPPING      | 1 : {ROW ADDR, BANK ADDR, COL ADDR} address mapping scheme<br>0 : {BANK ADDR, ROW ADDR, COL ADDR} address mapping scheme                                                                             | 0x0           |
| 28    | RW   | PWR_DOWN_EN      | 1 : Enable SDRAM precharge power down mode to save standby power. When enabled, SDRAM will go<br>0 : Disable SDRAM precharge power down mode                                                         | 0x0           |
| 27    | RW   | PWR_DOWN_MODE    | 1 : Active power down mode<br>0 : Precharge power down mode                                                                                                                                          | 0x0           |
| 26:25 | -    | -                | Reserved                                                                                                                                                                                             | 0x0           |
| 24    | RW   | SDRAM_WIDTH      | Number of SDRAM data bus bits :<br>0 : 16 bits(default)<br>1 : Reserved                                                                                                                              | 0x0           |
| 23:22 | -    | -                | Reserved                                                                                                                                                                                             | 0x0           |
| 21:20 | RW   | NUMCOLS          | Number of Column address bits :<br>0 : 8 Column address bits<br>1 : 9 Column address bits (default)<br>2 : 10 Column address bits<br>3: 11 Column address bits                                       | 0x1           |
| 19:18 | -    | -                | Reserved                                                                                                                                                                                             | 0x0           |
| 17:16 | RW   | NUMROWS          | Number of Row address bits :<br>0 : 11 Row address bits<br>1 : 12 Row address bits (default)<br>2 : 13 Row address bits<br>3: 14 Row address bits (not allocable if boot from NAND flash is enabled) | 0x2           |
| 15:0  | RW   | TREFR            | AUTO REFRESH period in number of SDRAM clock cycles – 1.                                                                                                                                             | 0x600         |

\*PS: SDRAM Self Refresh Mode and Power Down will be supported later.

**DRAM\_ARB\_CFG: DRAM arbiter configuration (offset: 0x0008)**

| Bits | Type | Name | Description | Initial value |
|------|------|------|-------------|---------------|
| 31   | -    | -    | Reserved    | 0x0           |

|       |    |                  |                                                                                                                                                                                        |       |
|-------|----|------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|
| 30    | RW | Round_Robin_EN   | Enable round-robin policy for arbiter<br>0: Disable<br>1: Enable                                                                                                                       | 0x0   |
| 29    | RW | CPU_POST_LOCK_EN | Enable arbiter to lock cpu for a while after service cpu<br>0: Disable<br>1: Enable                                                                                                    | 0x0   |
| 28    | RW | CPU_PRE_LOCK_EN  | Enable arbiter to lock cpu when detect the cpu command present in OCP bus<br>0: Disable<br>1: Enable                                                                                   | 0x0   |
| 27:16 | -  | 0                | Reserved                                                                                                                                                                               | 0x000 |
| 15:8  | RW | DMA_PENDING_CNT  | The counter is used to cancel the cpu lock when DMA request was pending for specified period clock count. The valid value is 1~255, "0" means to cancel the cpu pre/post lock function | 0x00  |
| 7:4   | -  | -                | Reserved                                                                                                                                                                               | 0x0   |
| 3:0   | RW | CPU_LOCK_CNT     | The counter is used to count the period of cpu post lock after service the cpu. The valid value is 1~15. "0" means post lock is 0 cycles                                               | 0x0   |

ILL\_ACC\_ADDR: Illegal Access Address Capture (offset: 0x0010)

| Bits | Type | Name         | Description                                                                                                                                                                                                                                                                                    | Initial value |
|------|------|--------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:0 | RO   | ILL_ACC_ADDR | If any bus masters (including CPU) issue illegal accesses (e.g. accessing to reserved memory space, non-double-word accessing to configuration registers), the address of the illegal transaction is captured in this register. An illegal interrupt will generate to indicate this exception. | 0x0           |

ILL\_ACC\_TYPE: Illegal Access TYPE Capture (offset: 0x0014)

| Bits  | Type | Name           | Description                                                                                                                                                                                                                                        | Initial value |
|-------|------|----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31    | W1C  | ILL_INT_STATUS | 1 : Indicate the illegal access interrupt is pending<br>0 : Indicate the illegal access interrupt is cleared<br>Write 1 to this bit will clear both ILL_ACC_ADDR and ILL_ACC_TYPE registers and thus clear the ILL_INT_STATUS.                     | 0x0           |
| 30    | RO   | ILL_ACC_WR     | Indicate the access type of the illegal access<br>1 : illegal access is write<br>0 : illegal access is read<br>This value is reset to 0 when ILL_ACC_ADDR is written                                                                               | 0x0           |
| 29:20 | -    | -              | Reserved                                                                                                                                                                                                                                           | 0x0           |
| 19:16 | RO   | ILL_ACC_BSEL   | Indicate the byte select of the illegal access<br>This value is reset to 0 when ILL_ACC_ADDR is written                                                                                                                                            | 0x0           |
| 15:11 | -    | -              | Reserved                                                                                                                                                                                                                                           | 0x0           |
| 10:8  | RO   | ILL_IID        | Indicate the initiator ID of the illegal access.<br>0 : CPU<br>1 : DMA<br>2 : PPE<br>3 : Ethernet PDMA RX<br>4 : Ethernet PDMA TX<br>5 : PCI/PCIE<br>6 : Embedded WLAN MAC/BBP<br>7 : USB<br>This value is reset to 0 when ILL_ACC_ADDR is written | 0x0           |
| 7:0   | RO   | ILL_ACC_LEN    | Indicate the access size of the illegal access. The unit is byte<br>This value is reset to 0 when ILL_ACC_ADDR is written.                                                                                                                         | 0x0           |



SDR\_PWR\_SAVE\_CNT: (offset: 0x001c)

| Bits  | Type | Name       | Description                                                                                                                                                                                                                                                                                                                                                                                                                           | Initial value |
|-------|------|------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:24 | RO   | PD_CNT     | A counter to show the times of entering self-refresh mode(only for DDR2)                                                                                                                                                                                                                                                                                                                                                              | 0x0           |
| 23:0  | RW   | SR_TAR_CNT | <p>This counter only was referenced when the SDR(PWR_DOWN_EN ) is set.</p> <p>This counter is use to count the period of the SDR IDLE status. When the IDLE period reach to the specified time period (SR_TAR_CNT*16/SYS_CLK_FREQ), the SDR will be automatically enter power saving or self-refresh mode. Software can configure it for suitable value.</p> <p>Here is reference table</p> <p>125MHz: 0x3ffff * 16* 8.0ns ~=46ms</p> | 0x3ffff       |

### 3.17 USB Host Controller & PHY

#### 3.17.1 Features

- Complies with the USB 2.0 Specification
- Host Controller Interface (OHCI) Specification, Version 1.0a.
- Supports ping and split transactions
- Descriptor and data prefetching.
- Complies with Enhanced Host Controller Interface (EHCI) Specification, Version 1.0, and the Open Host Controller Interface (OHCI) Specification, Version 1.0a.
- UTMI (legacy), UTMI+ to the PHY

#### 3.17.2 Block Diagram

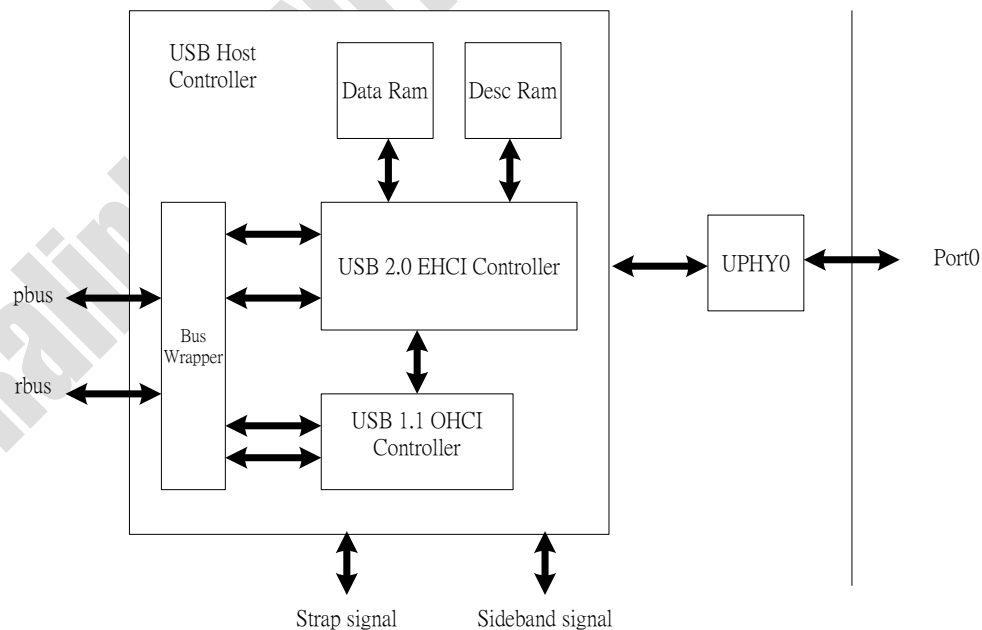


Fig. USB Host Controller & PHY Block Diagram

### 3.17.3 Register Description (base: 0x101c\_0000)

NOTE: To program EHCI and OHCI registers and initialize the core, refer to the Enhanced Host Controller Interface Specification for Universal Serial Bus and Open Host Controller Interface Specification for USB, respectively.

#### 3.17.3.1 EHCI Operation register (base: 0x101c\_0000)

##### EHCI Capability Register

| Mnemonic  | Register Name        | Offset From EHCI AHB Slave Start Address | Default Value                                                                                                                                                |
|-----------|----------------------|------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------|
| HCCAPBASE | Capability Register  | USBBASE <sup>1</sup> + 00h               | 32'h01000010                                                                                                                                                 |
| HCSPARAMS | Structural Parameter | USBBASE + 04h                            | 32'h00001116                                                                                                                                                 |
| HCCPARAMS | Capability Parameter | USBBASE + 08h                            | 32'h0000A010<br><b>Note:</b> The Isochronous Scheduling Threshold value is set to 1 by default. If Descriptor/Data Prefetch is selected, the value is set 2. |

USBBASE is fixed to EHCI slave start address = 0x101c\_0000

##### EHCI Operational Registers

| Mnemonic         | Register Name                             | Offset From EHCI AHB Slave Start Address <sup>1</sup> | Default Value                             |
|------------------|-------------------------------------------|-------------------------------------------------------|-------------------------------------------|
| USBCMD           | USB Command                               | USBOPBASE <sup>1</sup> + 00h                          | 32'h00080000 or 32'h00080B00 <sup>2</sup> |
| USBSTS           | USB Status                                | USBOPBASE + 04h                                       | 32'h00001000                              |
| USBINTR          | USB Interrupt Enable                      | USBOPBASE + 08h                                       | 32'h00000000                              |
| FRINDEX          | USB Frame Index                           | USBOPBASE + 0ch                                       | 32'h00000000                              |
| CTRLDSSEGMENT    | 4G Segment Selector                       | USBOPBASE + 10h                                       | 32'h00000000                              |
| PERIODICLISTBASE | Periodic Frame List Base Address Register | USBOPBASE + 14h                                       | 32'h00000000                              |
| ASYNCLISTADDR    | Asynchronous List Address                 | USBOPBASE + 18h                                       | 32'h00000000                              |

1. USBOPBASE is fixed to the EHCI slave start address + 'h10 (offset = 'h10).

2. The default value depends on whether Async park capability is enabled. Disabled = 32'h0008\_0000 and enabled = 32'h0008\_0B00.

The default value is:

32'h0008\_0000 if Async park capability is disabled (through coreConsultant)

32'h0008\_0B00 if Async park capability is enabled.

##### EHCI Auxiliary Power Well Registers

| Mnemonic              | Register Name            | Offset From EHCI AHB Slave Start Address | Default Value |
|-----------------------|--------------------------|------------------------------------------|---------------|
| CONFIGFLAG            | Configured Flag Register | USBOPBASE + 40h                          | 32'h00000000  |
| PORTSC_1 to PORTSC_15 | Port Status/Control      | USBOPBASE + 44h                          | 32'h00002000  |

—

— Support USB Host/Device Dual mode

- Complies with the On-The-Go Supplement to the USB 2.0 Specification (Revision 1.0a)
- Operates in High-Speed (HS, 480-Mbps), Full-Speed (FS, 12-Mbps) and Low-Speed (LS, 1.5-Mbps) modes
- Supports up to 4 bidirectional endpoints, including control endpoint 0
- Supports up to 4 host channels.
- Supports a generic root hub
- Includes automatic ping capabilities
- Supports Internal DMA modes
- Includes USB power management features
- Includes power-saving features (clock gating, two power rails for advanced power management)
- Supports packet-based, Dynamic FIFO memory allocation for endpoints for small FIFOs , and flexible, efficient use of RAM provides support to change an endpoint's FIFO memory size during transfers

**3.17.3.2 OHCI Operation register (base: 0x101c\_1000)**

| Offset   | 3                   | 0 |
|----------|---------------------|---|
|          | 1                   | 0 |
| 0        | HcRevision          |   |
| 4        | HcControl           |   |
| 8        | HcCommandStatus     |   |
| C        | HcInterruptStatus   |   |
| 10       | HcInterruptEnable   |   |
| 14       | HcInterruptDisable  |   |
| 18       | HcHCCA              |   |
| 1C       | HcPeriodCurrentED   |   |
| 20       | HcControlHeadED     |   |
| 24       | HcControlCurrentED  |   |
| 28       | HcBulkHeadED        |   |
| 2C       | HcBulkCurrentED     |   |
| 30       | HcDoneHead          |   |
| 34       | HcFmInterval        |   |
| 38       | HcFmRemaining       |   |
| 3C       | HcFmNumber          |   |
| 40       | HcPeriodicStart     |   |
| 44       | HcLSThreshold       |   |
| 48       | HcRhDescriptorA     |   |
| 4C       | HcRhDescriptorB     |   |
| 50       | HcRhStatus          |   |
| 54       | HcRhPortStatus[1]   |   |
| ...      | ...                 |   |
| 54+4*NDP | HcRhPortStatus[NDP] |   |

**3.18 USB Device Controller**
**3.18.1 Features**

- the USB 2.0 Specification (Revision 1.0a), operates in High-Speed (HS, 480-Mbps), Full-Speed (FS, 12-Mbps) and Low-Speed (LS, 1.5-Mbps) modes
- Supports up to 2 bulk-in and bulk out endpoints, including control endpoint 0
- Packet DMA (PDMA) is integrated for efficient data transfer.
- Support bulk-out aggregation features. More than one packet can be aggregated to single bulk transfer.
- Support two RX descriptor rings and two TX descriptor rings for QoS service.

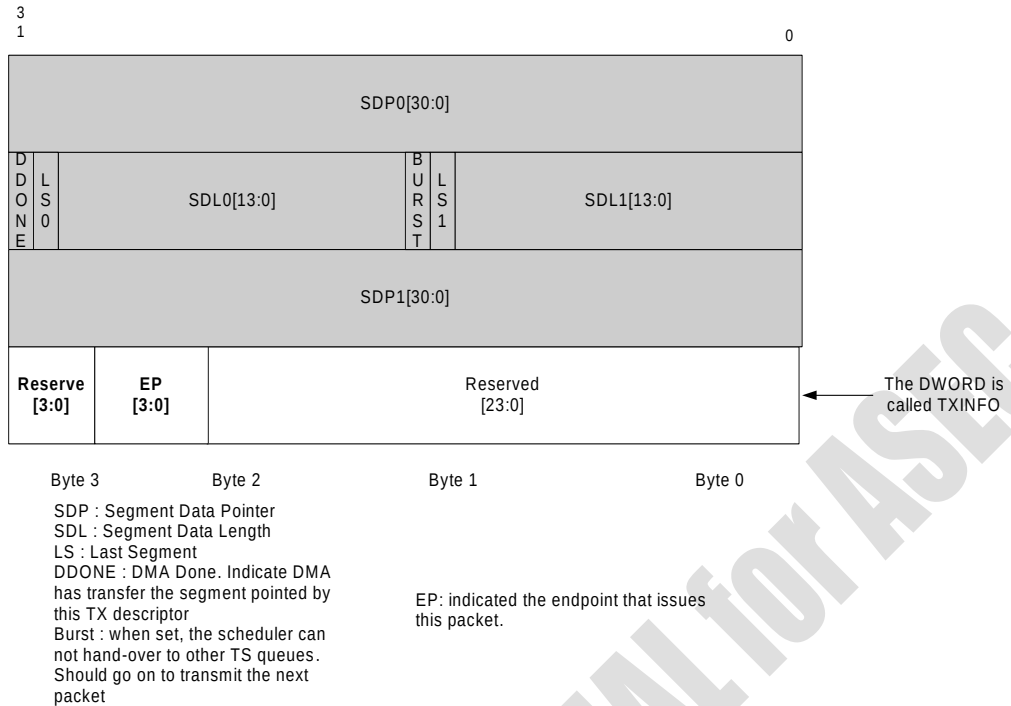
**3.18.1.1 PDMA descriptor format**


Fig. 3-12-3 PDMA TX descriptor format

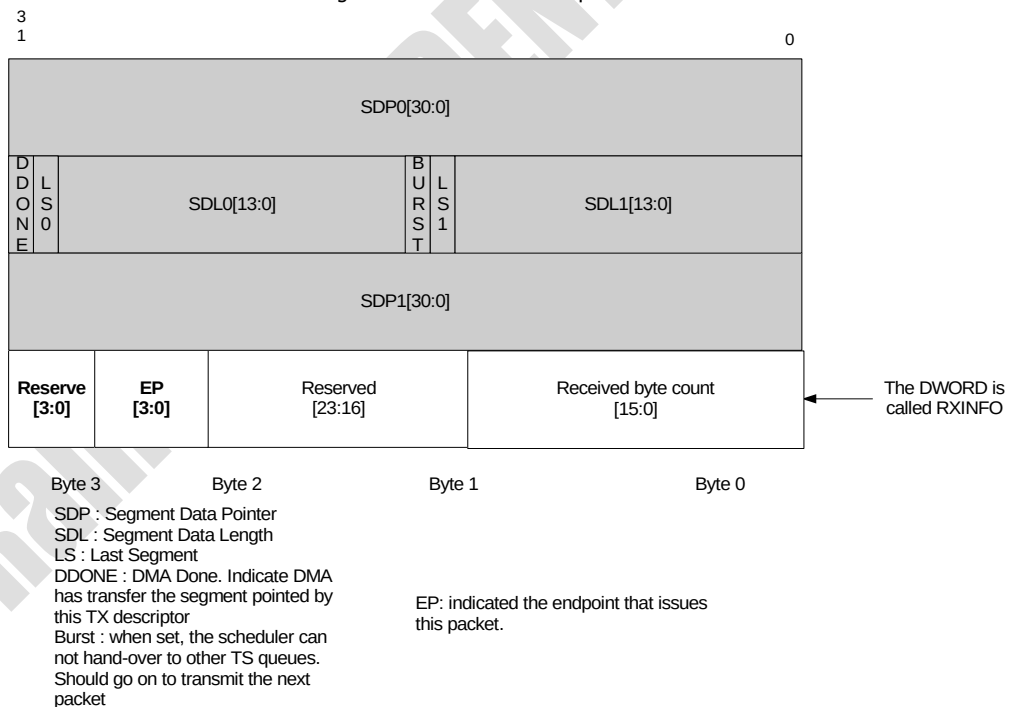
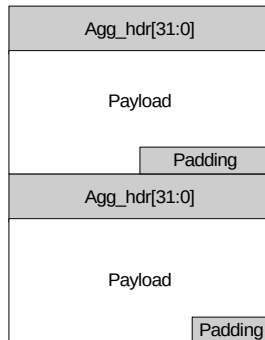


Fig. 3-12-4 PDMA RX descriptor format

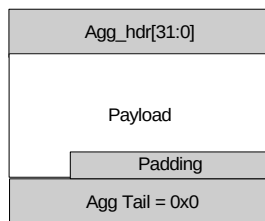
### 3.18.1.2 Bulk-out aggregation format

3  
1


Agg\_hdr[31:0]  
Agg\_hdr[31:16] reserved;  
Agg\_hdr[15:0] payload\_length;

Notice:

- 1) Each aggregation frame should add padding to align 4 byte boundary.
- 2) the payload\_length indicator the length of payload (no include padding)



### 3.18.2 Register Description (base: 0x1012\_0000)

#### 3.18.2.1 USB control registers

Refer to *case\_cusb2\_spec.pdf*.

**Registers address = Byte address \* 4.**

#### 3.18.2.2 UDMA registers

UDMA\_CTRL: (offset: 0x0800)

| Bits  | Type | Name         | Description                        | Initial value |
|-------|------|--------------|------------------------------------|---------------|
| 31:25 | -    | -            | Reserved                           | 0x0           |
| 24    | RW   | EPOUT1_DMAEN | EPOUT1 UDMA enable.                | 0x0           |
| 23:17 | -    | -            | Reserved                           | 0x0           |
| 16    | RW   | EPOUT1_AGGEN | EPOUT1 UDMA de-aggregation enable. | 0x0           |
| 15:10 | -    | -            | Reserved                           | 0x0           |
| 9:8   | RW   | EPOUT1_QSEL  | EPOUT1 Rx ring mapping.            | 0x0           |
| 7:5   | -    | -            | Reserved                           | 0x0           |
| 4     | RW   | WAKEUP_EN    | USB wakeup host enable.            | 0x0           |
| 3:2   | -    | -            | Reserved                           | 0x0           |
| 1     | RW   | UDMA_RX_EN   | UDMA Rx enable.                    | 0x0           |
| 0     | RW   | UDMA_TX_EN   | UDMA Tx enable.                    | 0x0           |

UDMA\_WRR: (offset: 0x0804)

| Bits  | Type | Name     | Description                | Initial value |
|-------|------|----------|----------------------------|---------------|
| 31:30 | -    | -        | Reserved                   | 0x0           |
| 29:28 | RW   | SCH_MODE | Scheduling mode<br>00: WRR | 0x0           |

|       |    |            |                                                                                                               |     |
|-------|----|------------|---------------------------------------------------------------------------------------------------------------|-----|
|       |    |            | 01: strict priority, EP1 > EP2 > EP3 > EP4 > EP5 > EP6<br>10: mixed mode, EP1 > EP2 > WRR(EP3, EP4, EP5, EP6) |     |
| 27:23 | -  | -          | Reserved                                                                                                      | 0x0 |
| 22:20 | RW | SCH_WT_EP6 | Scheduling weight of EPOUT6                                                                                   | 0x0 |
| 19    | -  | -          | Reserved                                                                                                      | 0x0 |
| 18:16 | RW | SCH_WT_EP5 | Scheduling weight of EPOUT5                                                                                   | 0x0 |
| 15    | -  | -          | Reserved                                                                                                      | 0x0 |
| 14:12 | RW | SCH_WT_EP4 | Scheduling weight of EPOUT4                                                                                   | 0x0 |
| 11    | -  | -          | Reserved                                                                                                      | 0x0 |
| 10:8  | RW | SCH_WT_EP3 | Scheduling weight of EPOUT3                                                                                   | 0x0 |
| 7     | -  | -          | Reserved                                                                                                      | 0x0 |
| 6:4   | RW | SCH_WT_EP2 | Scheduling weight of EPOUT2                                                                                   | 0x0 |
| 3     | -  | -          | Reserved                                                                                                      | 0x0 |
| 2:0   | RW | SCH_WT_EP1 | Scheduling weight of EPOUT1                                                                                   | 0x0 |

### 3.18.2.3 PDMA registers

TX\_RING\_NUM = 2

RX\_RING\_NUM = 2

TX\_BASE\_PTRn: (offset: 0x1000, 0x1010)

(n=0~TX\_RING\_NUM-1, offset = 0x1000 + n\*10)

| Bits  | Type | Name         | Description                                                     | Initial value |
|-------|------|--------------|-----------------------------------------------------------------|---------------|
| 31:16 | -    | -            | Reserved                                                        | 0x0           |
| 15:0  | RW   | TX_BASE_PTR0 | Point to the base address of TX_Ring0 (4-DWORD aligned address) | 0x0           |

TX\_MAX\_CNTn: (offset: 0x1004, 0x1014)

(n=0~TX\_RING\_NUM-1, offset = 0x1004 + n\*10)

| Bits | Type | Name        | Description                                   | Initial value |
|------|------|-------------|-----------------------------------------------|---------------|
| 31:8 | -    | -           | Reserved                                      | 0x0           |
| 7:0  | RW   | TX_MAX_CNT0 | The maximum number of TXD count in TXD_Ring0. | 0x0           |

TX\_CTX\_IDXn: (offset: 0x1008, 0x1018)

(n=0~TX\_RING\_NUM-1, offset = 0x1008 + n\*10)

| Bits | Type | Name        | Description                            | Initial value |
|------|------|-------------|----------------------------------------|---------------|
| 31:8 | -    | -           | Reserved                               | 0x0           |
| 7:0  | RW   | TX_CTX_IDX0 | Point to the next TXD CPU wants to use | 0x0           |

TX\_DTX\_IDXn: (offset: 0x100c, 0x101c)

(n=0~TX\_RING\_NUM-1, offset = 0x100c + n\*10)

| Bits | Type | Name        | Description                            | Initial value |
|------|------|-------------|----------------------------------------|---------------|
| 31:8 | -    | -           | Reserved                               | 0x0           |
| 7:0  | RO   | TX_DTX_IDX0 | Point to the next TXD DMA wants to use | 0x0           |

RX\_BASE\_PTR0: (offset: 0x1100, 0x1110)

(n=0~RX\_RING\_NUM-1, offset = 0x1100 + n\*10)

| Bits  | Type | Name         | Description                                                                                 | Initial value |
|-------|------|--------------|---------------------------------------------------------------------------------------------|---------------|
| 31:16 | -    | -            | Reserved                                                                                    | 0x0           |
| 15:0  | RW   | RX_BASE_PTR0 | Point to the base address of RXD Ring #0 (GE ports). It should be a 4-DWORD aligned address | 0x0           |

RX\_MAX\_CNT0: (offset: 0x1104, 0x1114)

(n=0~RX\_RING\_NUM-1, offset = 0x1104 + n\*10)

| Bits | Type | Name        | Description                                     | Initial value |
|------|------|-------------|-------------------------------------------------|---------------|
| 31:8 | -    | -           | Reserved                                        | 0x0           |
| 7:0  | RW   | RX_MAX_CNT0 | The maximum number of RXD count in RXD Ring #0. | 0x0           |

RX\_CALC\_IDX0: (offset: 0x1108, 0x1118)

(n=0~RX\_RING\_NUM-1, offset = 0x1100 + n\*10)

| Bits | Type | Name         | Description                                                 | Initial value |
|------|------|--------------|-------------------------------------------------------------|---------------|
| 31:8 | -    | -            | Reserved                                                    | 0x0           |
| 7:0  | RW   | RX_CALC_IDX0 | Point to the next RXD CPU wants to allocate to RXD Ring #0. | 0x0           |

FS\_DRX\_IDX0: (offset: 0x110c, 0x111c)

(n=0~RX\_RING\_NUM-1, offset = 0x1100 + n\*10)

| Bits | Type | Name        | Description                                                                                   | Initial value |
|------|------|-------------|-----------------------------------------------------------------------------------------------|---------------|
| 31:8 | -    | -           | Reserved                                                                                      | 0x0           |
| 7:0  | RW   | RX_DRX_IDX0 | Point to the next RXD DMA wants to use in FDS Ring#0. It should be a 4-DWORD aligned address. | 0x0           |

PDMA\_INFO: (offset:0x1200)

| Bits  | Type | Name           | Description                                                                                                                                                                                   | Initial value |
|-------|------|----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:28 | RO   | VERSION        | PDMA controller version.                                                                                                                                                                      | 0x1           |
| 27:24 | RO   | INDEX_WIDTH    | Ring index width                                                                                                                                                                              | 0xC           |
| 23:16 | RO   | BASE_PTR_WIDTH | Base pointer width, x<br>Base_addr[31:32-x] is shared with all ring base addr.<br>Only ring0's base address [31:32-x] field is writable.<br>PS: "0" is mean no bit of base_address is shared. | 0x0           |
| 15:8  | RO   | RX_RING_NUM    | Rx ring number                                                                                                                                                                                | 0x1           |
| 7:0   | RO   | TX_RING_NUM    | Tx ring number                                                                                                                                                                                | 0x2           |

PDMA\_GLO\_CFG: (offset:0x1204)

| Bits  | Type | Name        | Description                                                                                                                                                                                     | Initial value |
|-------|------|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:29 | -    | -           | Reserved                                                                                                                                                                                        | 0x0           |
| 28:16 | RW   | HDR_SEG_LEN | Specify the header segment size in byte to support RX header/payload scattering function, when set to a non-zero value.<br>When set to zero, the header/payload scattering feature is disabled. | 0x0           |
| 15:8  | -    | -           | Reserved                                                                                                                                                                                        | 0x0           |
| 7     | RW   | BIG_ENDIAN  | The endian mode selection. DMA applies the endian rule to convert payload and TX/RX information. DMA won't apply endian rule to register or descriptor. 1: big endian. 0: little endian.        | 0x0           |
| 6     | RW   | TX_WB_DDONE | 0 :Disable TX_DMA writing back DDONE into TXD<br>1 : Enable TX_DMA writing back DDONE into TXD                                                                                                  | 0x1           |



|   |    |               |                                                                                                                      |     |
|---|----|---------------|----------------------------------------------------------------------------------------------------------------------|-----|
| 5 | -  | -             | Reserved                                                                                                             | 0x0 |
| 4 | RW | WPDMA_BT_SIZE | Define the burst size of WPDMA<br>0 : 4 DWORD (16bytes)<br>1 : 8 DWORD (32 bytes)                                    | 0x1 |
| 3 | RO | RX_DMA_BUSY   | 1 : RX_DMA is busy<br>0 : RX_DMA is not busy                                                                         | 0x0 |
| 2 | RW | RX_DMA_EN     | 1 : Enable RX_DMA<br>0 : Disable RX_DMA (when disabled, RX_DMA will finish the current receiving packet, then stop.) | 0x0 |
| 1 | RO | TX_DMA_BUSY   | 1 : TX_DMA is busy<br>0 : TX_DMA is not busy                                                                         | 0x0 |
| 0 | RW | TX_DMA_EN     | 1 : Enable TX_DMA<br>0 : Disable TX_DMA (when disabled, TX_DMA will finish the current sending packet, then stop.)   | 0x0 |

**PDMA\_RST\_IDX: (offset:0x1208)**

| Bits  | Type | Name         | Description                            | Initial value |
|-------|------|--------------|----------------------------------------|---------------|
| 31:18 | -    | -            | Reserved                               | 0x0           |
| 17    | W1C  | RST_DRX_IDX1 | Write 1 to reset to RX_DMARX_IDX1 to 0 | 0x0           |
| 16    | W1C  | RST_DRX_IDX0 | Write 1 to reset to RX_DMARX_IDX0 to 0 | 0x0           |
| 15:2  | -    | -            | Reserved                               | 0x0           |
| 1     | W1C  | RST_DTX_IDX1 | Write 1 to reset to TX_DMATX_IDX1 to 0 | 0x0           |
| 0     | W1C  | RST_DTX_IDX0 | Write 1 to reset to TX_DMATX_IDX0 to 0 | 0x0           |

**DELAY\_INT\_CFG: (offset: 0x120c)**

| Bits  | Type | Name         | Description                                                                                                                                                                                                                                                                                    | Initial value |
|-------|------|--------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31    | RW   | TXDLY_INT_EN | 1: Enable TX delayed interrupt mechanism.<br>0: Disable TX delayed interrupt mechanism.                                                                                                                                                                                                        | 0x0           |
| 30:24 | RW   | TXMAX_PINT   | Specified Max # of pended interrupts.<br>When the # of pended interrupts equal or grater than the value specified here or interrupt pending time reach the limit (See bellow), an Final TX_DLY_INT is generated.<br><br>Set to 0 will disable pending interrupt count check                    | 0x0           |
| 23:16 | RW   | TXMAX_PTIME  | Specified Max pending time for the internal TX_DONE_INT0-5. When the pending time equal or grater TXMAX_PTIME x 20us or the # of pended TX_DONE_INT0-5 equal or grater than TXMAX_PINT (see above), an Final TX_DLY_INT is generated<br><br>Set to 0 will disable pending interrupt time check | 0x0           |
| 15    | RW   | RXDLY_INT_EN | 1: Enable RX delayed interrupt mechanism.<br>0: Disable RX delayed interrupt mechanism.                                                                                                                                                                                                        | 0x0           |
| 14:8  | RW   | RXMAX_PINT   | Specified Max # of pended interrupts.<br>When the # of pended interrupts equal or grater than the value specified here or interrupt pending time reach the limit (See bellow), an Final RX_DLY_INT is generated.<br><br>Set to 0 will disable pending interrupt count check                    | 0x0           |
| 7:0   | RW   | RXMAX_PTIME  | Specified Max pending time for the internal RX_DONE_INT. When the pending time equal or grater RXMAX_PTIME x 20us or , the # of pended RX_DONE_INT equal or grater than RXMAX_PCNT (see above), an Final RX_DLY_INT is generated                                                               | 0x0           |

|  |  |  |                                                    |  |
|--|--|--|----------------------------------------------------|--|
|  |  |  | Set to 0 will disable pending interrupt time check |  |
|--|--|--|----------------------------------------------------|--|

FREEQ\_THRES: (offset: 0x1210)

| Bits | Type | Name        | Description                                                         | Initial value |
|------|------|-------------|---------------------------------------------------------------------|---------------|
| 31:4 | -    | -           | Reserved                                                            | 0x0           |
| 3:0  | RW   | FreeQ_THRES | Will stop to block interface as RX-descriptors reach this threshold | 0x2           |

INT\_STATUS: (offset: 0x1220)

| Bits  | Type | Name         | Description                                                                                                                          | Initial value |
|-------|------|--------------|--------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31    | RW   | RX_COHERENT  | RX_DMA finds data coherent event when checking ddone bit.<br>Write 1 to clear the interrupt.<br>Read to get the raw interrupt status | 0x0           |
| 30    | RW   | RX_DLY_INT   | Summary of the whole WPDMA RX related interrupts<br>Write 1 to clear the interrupt.<br>Read to get the raw interrupt status          | 0x0           |
| 29    | RW   | TX_COHERENT  | TX_DMA finds data coherent event when checking ddone bit.<br>Write 1 to clear the interrupt.<br>Read to get the raw interrupt status | 0x0           |
| 28    | RW   | TX_DLY_INT   | Summary of the whole WPDMA TX related interrupts<br>Write 1 to clear the interrupt.<br>Read to get the raw interrupt status          | 0x0           |
| 27:18 | -    | -            | Reserved                                                                                                                             | 0x0           |
| 17    | RW   | RX_DONE_INT1 | RX Queue#1 packet receive interrupt<br>Write 1 to clear the interrupt.<br>Read to get the raw interrupt status                       | 0x0           |
| 16    | RW   | RX_DONE_INT0 | RX Queue#0 packet receive interrupt<br>Write 1 to clear the interrupt.<br>Read to get the raw interrupt status                       | 0x0           |
| 15:2  | -    | -            | Reserved                                                                                                                             | 0x0           |
| 1     | RW   | TX_DONE_INT1 | TX Queue#1 packet transmit interrupt<br>Write 1 to clear the interrupt.<br>Read to get the raw interrupt status                      | 0x0           |
| 0     | RW   | TX_DONE_INT0 | TX Queue#0 packet transmit interrupt<br>Write 1 to clear the interrupt.<br>Read to get the raw interrupt status                      | 0x0           |

INT\_MASK: (offset: 0x1228)

| Bits | Type | Name                | Description                                                                                               | Initial value |
|------|------|---------------------|-----------------------------------------------------------------------------------------------------------|---------------|
| 31   | RW   | RX_COHERENT_INT_MSK | Interrupt enable for RX_DMA data coherent event..<br>1: Enable the interrupt<br>0: Disable the interrupt  | 0x0           |
| 30   | RW   | RX_DLY_INT_MSK      | Summary of the whole WPDMA RX related interrupts<br>1 : Enable the interrupt<br>0 : Disable the interrupt | 0x0           |
| 29   | RW   | TX_COHERENT_INT_MSK | Interrupt enable for TX_DMA data coherent event..<br>1: Enable the interrupt<br>0: Disable the interrupt  | 0x0           |
| 28   | RW   | TX_DLY_INT_MSK      | Summary of the whole WPDMA TX related interrupts<br>1 : Enable the interrupt                              | 0x0           |

|       |    |                  |                                                                                               |     |
|-------|----|------------------|-----------------------------------------------------------------------------------------------|-----|
|       |    |                  | 0 : Disable the interrupt                                                                     |     |
| 27:18 | -  | -                | Reserved                                                                                      | 0x0 |
| 17    | RW | RX_DONE_INT_MSK1 | RX Queue#1 packet receive interrupt<br>1 : Enable the interrupt<br>0 : Disable the interrupt  | 0x0 |
| 16    | RW | RX_DONE_INT_MSK0 | RX Queue#0 packet receive interrupt<br>1 : Enable the interrupt<br>0 : Disable the interrupt  | 0x0 |
| 15:2  | -  | -                | Reserved                                                                                      | 0x0 |
| 1     | RW | TX_DONE_INT_MSK1 | TX Queue#1 packet transmit interrupt<br>1 : Enable the interrupt<br>0 : Disable the interrupt | 0x0 |
| 0     | RW | TX_DONE_INT_MSK0 | TX Queue#0 packet transmit interrupt<br>1 : Enable the interrupt<br>0 : Disable the interrupt | 0x0 |

**PDMA\_SCH: (offset: 0x1280)**

| Bits  | Type | Name     | Description                                                                                                                                           | Initial value |
|-------|------|----------|-------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:26 | -    | -        | Reserved                                                                                                                                              | -             |
| 25:24 | RW   | SCH_MODE | Scheduling mode<br>00: WRR<br>01: Strict priority, Q3 > Q2 > Q1 > Q0<br>10: Mixed mode, Q3 > WRR(Q2, Q1, Q0)<br>11: Mixed mode, Q3 > Q2 > WRR(Q1, Q0) | 0x0           |
| 23:0  | -    | -        | Reserved                                                                                                                                              | -             |

**PDMA\_WRR: (offset: 0x1284)**

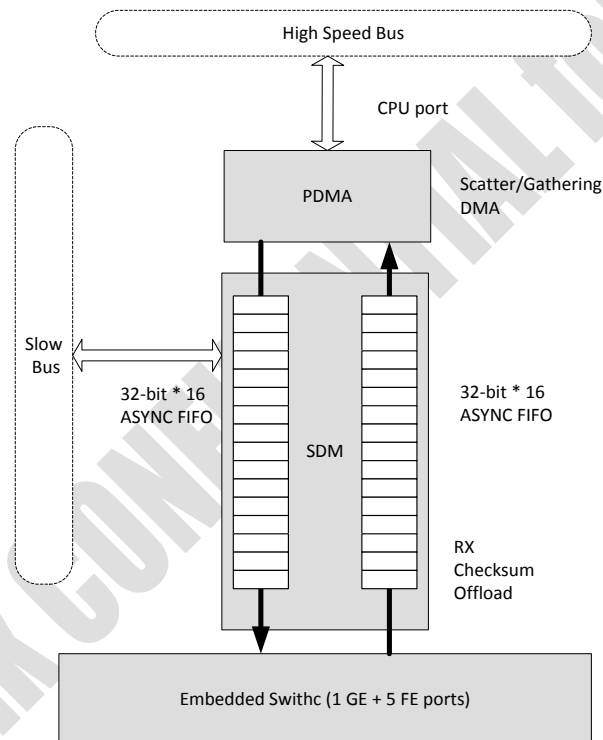
| Bits  | Type | Name      | Description                | Initial value |
|-------|------|-----------|----------------------------|---------------|
| 31:15 | -    | -         | Reserved                   | -             |
| 14:12 | RW   | SCH_WT_Q3 | Scheduling weight of Tx Q3 | 0x0           |
| 11    | -    | -         | Reserved                   | -             |
| 10:8  | RW   | SCH_WT_Q2 | Scheduling weight of Tx Q2 | 0x0           |
| 7     | -    | -         | Reserved                   | -             |
| 6:4   | RW   | SCH_WT_Q1 | Scheduling weight of Tx Q1 | 0x0           |
| 3     | -    | -         | Reserved                   | -             |
| 2:0   | RW   | SCH_WT_Q0 | Scheduling weight of Tx Q0 | 0x0           |

### 3.19 Frame Engine

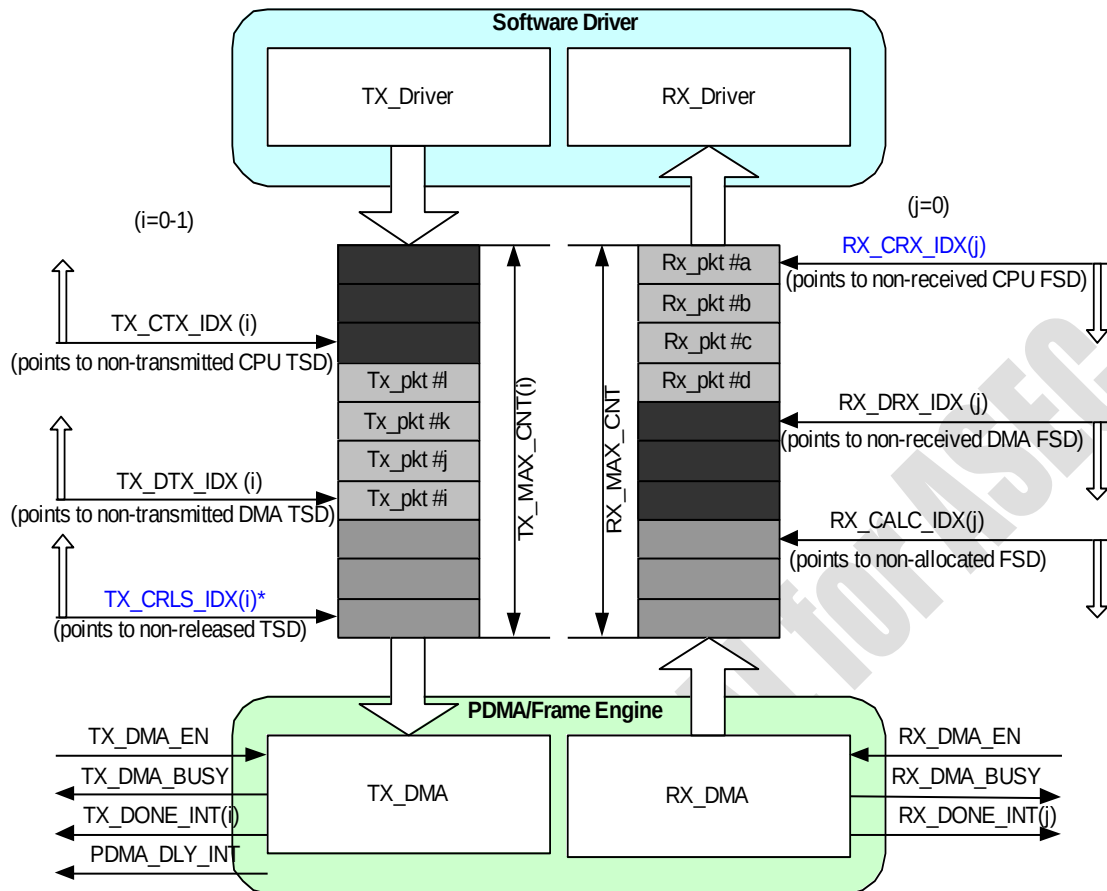
#### 3.19.1 Features

- Supports 4 TX descriptor rings and 2 RX descriptor ring
- Scatter/Gather DMA
- Delayed interrupt
- Configurable 4/8 double-word burst length
- Configurable TX/RX flow control mechanism
- Frames separated to 2 RX ring by Priority tag or Source port
- RX Checksum offload
- TX/RX Counters for debug

#### 3.19.2 Block Diagram



##### 3.19.2.1 PDMA FIFO-like Ring Concept



Note 1 : TX\_CRLS\_IDX(i) and RX\_CRX\_IDX (j) are not in PDMA hardware, they are resident in CPU local memory

Note 2:

TXQ0 : GE MAC low priority queue  
TXQ1 : GE MAC high priority queue

RXQ0 : For GE MAC receive

Fig. 3-12-2 PDMA FIFO-like ring concept

### 3.19.2.2 PDMA Descriptor Format

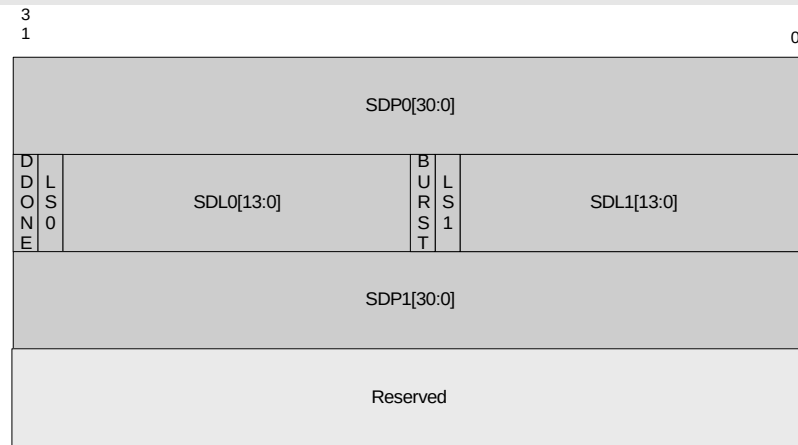


Fig. 3-12-3 PDMA TX descriptor format

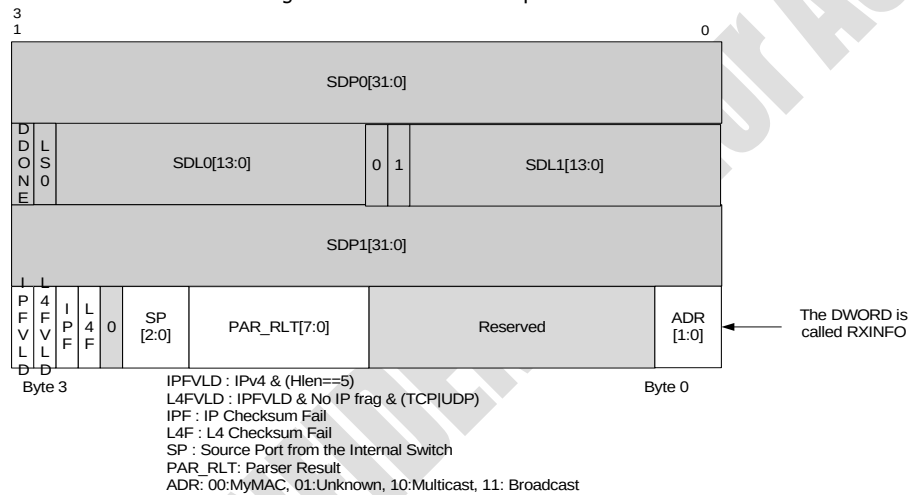


Fig. 3-12-4 PDMA RX descriptor format

Fig. 3-12 EEPROM/EFUSE controller Block Diagram

### 3.19.3 PDMA Register Description(base: 0x1010\_0800)

TX\_BASE\_PTRn: (offset: 0x0000, 0x0010, 0x0020, 0x0030)(n: 0~3)

| Bits  | Type | Name        | Description                                                     | Initial value |
|-------|------|-------------|-----------------------------------------------------------------|---------------|
| 31:16 | -    | -           | Reserved                                                        | -             |
| 15:0  | RW   | TX_BASE_PTR | Point to the base address of TX_Ring0 (4-DWORD aligned address) | 0x0           |

TX\_MAX\_CNTn: (offset: 0x0004, 0x0014, 0x0024, 0x0034)(n: 0~3)

| Bits | Type | Name       | Description                                   | Initial value |
|------|------|------------|-----------------------------------------------|---------------|
| 31:8 | -    | -          | Reserved                                      | -             |
| 7:0  | RW   | TX_MAX_CNT | The maximum number of TXD count in TXD_Ring0. | 0x0           |

TX\_CTX\_IDXn: (offset: 0x0008, 0x0018, 0x0028, 0x0038)(n: 0~3)

| Bits | Type | Name | Description | Initial value |
|------|------|------|-------------|---------------|
| 31:8 | -    | -    | Reserved    | -             |

|     |    |            |                                        |     |
|-----|----|------------|----------------------------------------|-----|
| 7:0 | RW | TX_CTX_IDX | Point to the next TXD CPU wants to use | 0x0 |
|-----|----|------------|----------------------------------------|-----|

TX\_DTX\_IDXn: (offset: 0x000c, 0x001c, 0x002c, 0x003c)(n: 0~3)

| Bits | Type | Name       | Description                            | Initial value |
|------|------|------------|----------------------------------------|---------------|
| 31:8 | -    | -          | Reserved                               | -             |
| 7:0  | RO   | TX_DTX_IDX | Point to the next TXD DMA wants to use | 0x0           |

RX\_BASE\_PTRn: (offset: 0x0100, 0x0110)(n: 0~1)

| Bits  | Type | Name        | Description                                                                                 | Initial value |
|-------|------|-------------|---------------------------------------------------------------------------------------------|---------------|
| 31:16 | -    | -           | Reserved                                                                                    | -             |
| 15:0  | RW   | RX_BASE_PTR | Point to the base address of RXD Ring #0 (GE ports). It should be a 4-DWORD aligned address | 0x0           |

RX\_MAX\_CNTn: (offset: 0x0104, 0x0114)(n: 0~1)

| Bits | Type | Name       | Description                                     | Initial value |
|------|------|------------|-------------------------------------------------|---------------|
| 31:8 | -    | -          | Reserved                                        | -             |
| 7:0  | RW   | RX_MAX_CNT | The maximum number of RXD count in RXD Ring #0. | 0x0           |

RX\_CALC\_IDXn: (offset: 0x0108, 0x0118)(n: 0~1)

| Bits | Type | Name         | Description                                                 | Initial value |
|------|------|--------------|-------------------------------------------------------------|---------------|
| 31:8 | -    | -            | Reserved                                                    | -             |
| 7:0  | RW   | RX_CALC_IDX0 | Point to the next RXD CPU wants to allocate to RXD Ring #0. | 0x0           |

RX\_DRX\_IDXn: (offset: 0x010c, 0x011c)(n: 0~1)

| Bits | Type | Name        | Description                                                                                   | Initial value |
|------|------|-------------|-----------------------------------------------------------------------------------------------|---------------|
| 31:8 | -    | -           | Reserved                                                                                      | -             |
| 7:0  | RW   | RX_DRX_IDX0 | Point to the next RXD DMA wants to use in RXD Ring#0. It should be a 4-DWORD aligned address. | 0x0           |

PDMA\_INFO: (offset: 0x0200)

| Bits  | Type | Name           | Description                                                                                                                                                                                   | Initial value |
|-------|------|----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:28 | RO   | VERSION        | PDMA controller version.                                                                                                                                                                      | 0x1           |
| 27:24 | RO   | INDEX_WIDTH    | Ring index width                                                                                                                                                                              | 0xC           |
| 23:16 | RO   | BASE_PTR_WIDTH | Base pointer width, x<br>Base_addr[31:32-x] is shared with all ring base addr.<br>Only ring0's base address [31:32-x] field is writable.<br>PS: "0" is mean no bit of base_address is shared. | 0x0           |
| 15:8  | RO   | RX_RING_NUM    | Rx ring number                                                                                                                                                                                | 0x2           |
| 7:0   | RO   | TX_RING_NUM    | Tx ring number                                                                                                                                                                                | 0x4           |

PDMA\_GLO\_CFG: (offset: 0x0204)

| Bits  | Type | Name        | Description                                                                                                                                                                                     | Initial value |
|-------|------|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:29 | -    | -           | Reserved                                                                                                                                                                                        | -             |
| 28:16 | RW   | HDR_SEG_LEN | Specify the header segment size in byte to support RX header/payload scattering function, when set to a non-zero value.<br>When set to zero, the header/payload scattering feature is disabled. | 0x0           |
| 15:8  | -    | -           | Reserved                                                                                                                                                                                        | -             |
| 7     | RW   | BIG_ENDIAN  | The endian mode selection. DMA applies the endian rule to convert payload and TX/RX information. DMA won't apply                                                                                | 0x0           |

|   |    |               |                                                                                                                      |     |
|---|----|---------------|----------------------------------------------------------------------------------------------------------------------|-----|
|   |    |               | endian rule to register or descriptor. 1: big endian. 0: little endian.                                              |     |
| 6 | RW | TX_WB_DDONE   | 0 : Disable TX_DMA writing back DDONE into TXD<br>1 : Enable TX_DMA writing back DDONE into TXD                      | 0x1 |
| 5 | -  | -             | Reserved                                                                                                             | -   |
| 4 | RW | WPDMA_BT_SIZE | Define the burst size of WPDMA<br>0 : 4 DWORD (16bytes)<br>1 : 8 DWORD (32 bytes)                                    | 0x1 |
| 3 | RO | RX_DMA_BUSY   | 1 : RX_DMA is busy<br>0 : RX_DMA is not busy                                                                         | 0x0 |
| 2 | RW | RX_DMA_EN     | 1 : Enable RX_DMA<br>0 : Disable RX_DMA (when disabled, RX_DMA will finish the current receiving packet, then stop.) | 0x0 |
| 1 | RO | TX_DMA_BUSY   | 1 : TX_DMA is busy<br>0 : TX_DMA is not busy                                                                         | 0x0 |
| 0 | RW | TX_DMA_EN     | 1 : Enable TX_DMA<br>0 : Disable TX_DMA (when disabled, TX_DMA will finish the current sending packet, then stop.)   | 0x0 |

**PDMA\_RST\_IDX: (offset: 0x0208)**

| Bits  | Type | Name         | Description                            | Initial value |
|-------|------|--------------|----------------------------------------|---------------|
| 31:18 | -    | -            | Reserved                               | -             |
| 17    | W1C  | RST_DRX_IDX1 | Write 1 to reset to RX_DMARX_IDX1 to 0 | 0x0           |
| 16    | W1C  | RST_DRX_IDX0 | Write 1 to reset to RX_DMARX_IDX0 to 0 | 0x0           |
| 15:4  | -    | -            | Reserved                               | -             |
| 3     | W1C  | RST_DTX_IDX3 | Write 1 to reset to TX_DMATX_IDX3 to 0 | 0x0           |
| 2     | W1C  | RST_DTX_IDX2 | Write 1 to reset to TX_DMATX_IDX2 to 0 | 0x0           |
| 1     | W1C  | RST_DTX_IDX1 | Write 1 to reset to TX_DMATX_IDX1 to 0 | 0x0           |
| 0     | W1C  | RST_DTX_IDX0 | Write 1 to reset to TX_DMATX_IDX0 to 0 | 0x0           |

**DELAY\_INT\_CFG: (offset: 0x020c)**

| Bits  | Type | Name         | Description                                                                                                                                                                                                                                                                                    | Initial value |
|-------|------|--------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31    | RW   | TXDLY_INT_EN | 1: Enable TX delayed interrupt mechanism.<br>0: Disable TX delayed interrupt mechanism.                                                                                                                                                                                                        | 0x0           |
| 30:24 | RW   | TXMAX_PINT   | Specified Max # of pended interrupts.<br>When the # of pended interrupts equal or grater than the value specified here or interrupt pending time reach the limit (See bellow), an Final TX_DLY_INT is generated.<br><br>Set to 0 will disable pending interrupt count check                    | 0x0           |
| 23:16 | RW   | TXMAX_PTIME  | Specified Max pending time for the internal TX_DONE_INT0-5. When the pending time equal or grater TXMAX_PTIME x 20us or the # of pended TX_DONE_INT0-5 equal or grater than TXMAX_PINT (see above), an Final TX_DLY_INT is generated<br><br>Set to 0 will disable pending interrupt time check | 0x0           |
| 15    | RW   | RXDLY_INT_EN | 1: Enable RX delayed interrupt mechanism.<br>0: Disable RX delayed interrupt mechanism.                                                                                                                                                                                                        | 0x0           |
| 14:8  | RW   | RXMAX_PINT   | Specified Max # of pended interrupts.<br>When the # of pended interrupts equal or grater than the value specified here or interrupt pending time reach the limit (See bellow), an Final RX_DLY_INT is generated.                                                                               | 0x0           |



|     |    |             |                                                                                                                                                                                                                                                                                               |     |
|-----|----|-------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|
|     |    |             | Set to 0 will disable pending interrupt count check                                                                                                                                                                                                                                           |     |
| 7:0 | RW | RXMAX_PTIME | Specified Max pending time for the internal RX_DONE_INT.<br>When the pending time equal or grater RXMAX_PTIME x 20us or , the # of pended RX_DONE_INT equal or grater than RXMAX_PCNT (see above), an Final RX_DLY_INT is generated<br><br>Set to 0 will disable pending interrupt time check | 0x0 |

**FREEQ\_THRES: (offset: 0x0210)**

| Bits | Type | Name        | Description                                                         | Initial value |
|------|------|-------------|---------------------------------------------------------------------|---------------|
| 31:4 | -    | -           | Reserved                                                            | -             |
| 3:0  | RW   | FreeQ_THRES | Will stop to block interface as RX-descriptors reach this threshold | 0x2           |

**INT\_STATUS: (offset: 0x0220)**

| Bits  | Type | Name         | Description                                                                                                                          | Initial value |
|-------|------|--------------|--------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31    | RW   | RX_COHERENT  | RX_DMA finds data coherent event when checking ddone bit.<br>Write 1 to clear the interrupt.<br>Read to get the raw interrupt status | 0x0           |
| 30    | RW   | RX_DLY_INT   | Summary of the whole WPDMA RX related interrupts<br>Write 1 to clear the interrupt.<br>Read to get the raw interrupt status          | 0x0           |
| 29    | RW   | TX_COHERENT  | TX_DMA finds data coherent event when checking ddone bit.<br>Write 1 to clear the interrupt.<br>Read to get the raw interrupt status | 0x0           |
| 28    | RW   | TX_DLY_INT   | Summary of the whole WPDMA TX related interrupts<br>Write 1 to clear the interrupt.<br>Read to get the raw interrupt status          | 0x0           |
| 27:18 | -    | -            | Reserved                                                                                                                             | -             |
| 17    | RW   | RX_DONE_INT1 | RX Queue#1 packet receive interrupt<br>Write 1 to clear the interrupt.<br>Read to get the raw interrupt status                       | 0x0           |
| 16    | RW   | RX_DONE_INT0 | RX Queue#0 packet receive interrupt<br>Write 1 to clear the interrupt.<br>Read to get the raw interrupt status                       | 0x0           |
| 15:4  | -    | -            | Reserved                                                                                                                             | -             |
| 3     | RW   | TX_DONE_INT3 | TX Queue#3 packet transmit interrupt<br>Write 1 to clear the interrupt.<br>Read to get the raw interrupt status                      | 0x0           |
| 2     | RW   | TX_DONE_INT2 | TX Queue#2 packet transmit interrupt<br>Write 1 to clear the interrupt.<br>Read to get the raw interrupt status                      | 0x0           |
| 1     | RW   | TX_DONE_INT1 | TX Queue#1 packet transmit interrupt<br>Write 1 to clear the interrupt.<br>Read to get the raw interrupt status                      | 0x0           |
| 0     | RW   | TX_DONE_INT0 | TX Queue#0 packet transmit interrupt<br>Write 1 to clear the interrupt.<br>Read to get the raw interrupt status                      | 0x0           |

INT\_MASK: (offset: 0x0228)

| Bits  | Type | Name                | Description                                                                                               | Initial value |
|-------|------|---------------------|-----------------------------------------------------------------------------------------------------------|---------------|
| 31    | RW   | RX_COHERENT_INT_MSK | Interrupt enable for RX_DMA data coherent event..<br>1: Enable the interrupt<br>0: Disable the interrupt  | 0x0           |
| 30    | RW   | RX_DLY_INT_MSK      | Summary of the whole WPDMA RX related interrupts<br>1 : Enable the interrupt<br>0 : Disable the interrupt | 0x0           |
| 29    | RW   | TX_COHERENT_INT_MSK | Interrupt enable for TX_DMA data coherent event..<br>1: Enable the interrupt<br>0: Disable the interrupt  | 0x0           |
| 28    | RW   | TX_DLY_INT_MSK      | Summary of the whole WPDMA TX related interrupts<br>1 : Enable the interrupt<br>0 : Disable the interrupt | 0x0           |
| 27:18 | -    | -                   | Reserved                                                                                                  | -             |
| 17    | RW   | RX_DONE_INT_MSK1    | RX Queue#1 packet receive interrupt<br>1 : Enable the interrupt<br>0 : Disable the interrupt              | 0x0           |
| 16    | RW   | RX_DONE_INT_MSK0    | RX Queue#0 packet receive interrupt<br>1 : Enable the interrupt<br>0 : Disable the interrupt              | 0x0           |
| 15:2  | -    | -                   | Reserved                                                                                                  | -             |
| 3     | RW   | TX_DONE_INT_MSK3    | TX Queue#3 packet transmit interrupt<br>1 : Enable the interrupt<br>0 : Disable the interrupt             | 0x0           |
| 2     | RW   | TX_DONE_INT_MSK2    | TX Queue#2 packet transmit interrupt<br>1 : Enable the interrupt<br>0 : Disable the interrupt             | 0x0           |
| 1     | RW   | TX_DONE_INT_MSK1    | TX Queue#1 packet transmit interrupt<br>1 : Enable the interrupt<br>0 : Disable the interrupt             | 0x0           |
| 0     | RW   | TX_DONE_INT_MSK0    | TX Queue#0 packet transmit interrupt<br>1 : Enable the interrupt<br>0 : Disable the interrupt             | 0x0           |

PDMA\_SCH: (offset: 0x0280)

| Bits  | Type | Name     | Description                                                                                                                                           | Initial value |
|-------|------|----------|-------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:26 | -    | -        | Reserved                                                                                                                                              | -             |
| 25:24 | RW   | SCH_MODE | Scheduling mode<br>00: WRR<br>01: Strict priority, Q3 > Q2 > Q1 > Q0<br>10: Mixed mode, Q3 > WRR(Q2, Q1, Q0)<br>11: Mixed mode, Q3 > Q2 > WRR(Q1, Q0) | 0x0           |
| 23:0  | -    | -        | Reserved                                                                                                                                              | -             |

PDMA\_WRR: (offset: 0x0284)

| Bits  | Type | Name      | Description                | Initial value |
|-------|------|-----------|----------------------------|---------------|
| 31:15 | -    | -         | Reserved                   | -             |
| 14:12 | RW   | SCH_WT_Q3 | Scheduling weight of Tx Q3 | 0x0           |

|      |    |           |                            |     |
|------|----|-----------|----------------------------|-----|
| 11   | -  | -         | Reserved                   | -   |
| 10:8 | RW | SCH_WT_Q2 | Scheduling weight of Tx Q2 | 0x0 |
| 7    | -  | -         | Reserved                   | -   |
| 6:4  | RW | SCH_WT_Q1 | Scheduling weight of Tx Q1 | 0x0 |
| 3    | -  | -         | Reserved                   | -   |
| 2:0  | RW | SCH_WT_Q0 | Scheduling weight of Tx Q0 | 0x0 |

### 3.19.4 SDM Register Description(base: 0x1010\_0c00)

SDM\_CON: Switch DMA Configuration Register(offset: 0x0000)

| Bits  | Type | Name       | Description                                                                                                                                                                                                     | Initial value |
|-------|------|------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:24 | -    | -          | Reserved                                                                                                                                                                                                        | -             |
| 23    | RW   | PDMA_FC    | TX PDMA Flow-Control Enable<br>When this bit is set, the downstream flow-control is enabled on PDMA 4 TX Ring (SDM_TRING).<br>0: Disable<br>1: Enable                                                           | 0x0           |
| 22    | RW   | PORT_MAP   | RX Ring Selection<br>The received frame will be collected into the corresponding PDMA RX Ring based on the source port or priority tag.<br>0: Priority Tag (SDM_RRING[7:0])<br>1: Source Port (SDM_RRING[12:8]) | 0x0           |
| 21    | RW   | LOOP_EN    | Frame Engine Loop-back Mode Enable<br>When this bit is set, the received frame by the frame engine will be forwarded directly to the internal switch without modification.                                      | 0x0           |
| 20    | RW   | TCI_81XX   | Special Tag Recongization Enable<br>When this bit is set, PID(0x8100) is recognized by the first byte (0x81) only. The second byte could be used for special purpose like the incoming source port.             | 0x0           |
| 19    | RW   | UN_DROR_EN | Drop Unknown MAC Addresss<br>0: disable<br>1: enable                                                                                                                                                            | 0x0           |
| 18    | RW   | UDPCS      | UDP Packet Checksum RX Offload Enable<br>0: disable, checksum result is showed on RX descriptor<br>1: enable, drop checksum error packet                                                                        | 0x1           |
| 17    | RW   | TCPCS      | TCP Packet Chekcsum RX Offload Enable<br>0: disable, checksum result is showed on RX descriptor<br>1: enable, drop checksum error packet                                                                        | 0x1           |
| 16    | RW   | IPCS       | IP Header Checksum RX Offload Enable<br>0: disable, checksum result is showed on RX descriptor<br>1: enable, drop checksum error packet                                                                         | 0x1           |
| 15:0  | RW   | EXT_VLAN   | Outer VLAN Protocol ID<br>The specific value is used to recognize the outer VLAN protocol ID only. Per inner VLAN or the general VLAN-tagged frame, the value PID=0x8100 is the unique Protocol ID.             | 0x8100        |

SDM\_RRING: Switch DMA RX Ring Register(offset: 0x0004)

| Bits  | Type | Name         | Description                                                                                                                                                                                                                | Initial value |
|-------|------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:20 | -    | -            | Reserved                                                                                                                                                                                                                   | -             |
| 19    | RW   | QUE3_RING_FC | Pause Switch Queue 3 by RX Ring#<br>When Rx Ring# reaches the reserved free threshold (FREEQ_THRES) , the queue 3 to CPU will be paused.<br>0: RX Ring #0<br>1: RX Ring #1                                                 | 0x0           |
| 18    | RW   | QUE2_RING_FC | Pause Switch Queue 2 by RX Ring#<br>0: RX Ring #0<br>1: RX Ring #1                                                                                                                                                         | 0x0           |
| 17    | RW   | QUE1_RING_FC | Pause Switch Queue 1 by RX Ring#<br>0: RX Ring #0<br>1: RX Ring #1                                                                                                                                                         | 0x0           |
| 16    | RW   | QUE0_RING_FC | Pause Switch Queue 0 by RX Ring#<br>0: RX Ring #0<br>1: RX Ring #1                                                                                                                                                         | 0x0           |
| 15:13 | -    | -            | Reserved                                                                                                                                                                                                                   | -             |
| 12    | RW   | PORT4_RING   | Source Port 4 to RX Ring#<br>The received frames from the source port 4 will be sent to RX Ring#<br>(Note: To use the source port, the special tag between FE and SW should be enabled.)<br>0: RX Ring #0<br>1: RX Ring #1 | 0x0           |
| 11    | RW   | PORT3_RING   | Source Port 3 to RX Ring#<br>0: RX Ring #0<br>1: RX Ring #1                                                                                                                                                                | 0x0           |
| 10    | RW   | PORT2_RING   | Source Port 2 to RX Ring#<br>0: RX Ring #0<br>1: RX Ring #1                                                                                                                                                                | 0x0           |
| 9     | RW   | PORT1_RING   | Source Port 1 to RX Ring#<br>0: RX Ring #0<br>1: RX Ring #1                                                                                                                                                                | 0x0           |
| 8     | RW   | PORT0_RING   | Source Port 0 to RX Ring#<br>0: RX Ring #0<br>1: RX Ring #1                                                                                                                                                                | 0x0           |
| 7     | RW   | PRI7_RING    | Priority 7 to RX Ring#<br>The received frames with priority tag 7 will be sent to RX Ring#<br>0: RX Ring #0<br>1: RX Ring #1                                                                                               | 0x0           |
| 6     | RW   | PRI6_RING    | Priority 6 to RX Ring#<br>0: RX Ring #0<br>1: RX Ring #1                                                                                                                                                                   | 0x0           |
| 5     | RW   | PRI5_RING    | Priority 5 to RX Ring#<br>0: RX Ring #0<br>1: RX Ring #1                                                                                                                                                                   | 0x0           |
| 4     | RW   | PRI4_RING    | Priority 4 to RX Ring#<br>0: RX Ring #0                                                                                                                                                                                    | 0x0           |

|   |    |           |                                                          |     |
|---|----|-----------|----------------------------------------------------------|-----|
|   |    |           | 1: RX Ring #1                                            |     |
| 3 | RW | PRI3_RING | Priority 3 to RX Ring#<br>0: RX Ring #0<br>1: RX Ring #1 | 0x0 |
| 2 | RW | PRI2_RING | Priority 2 to RX Ring#<br>0: RX Ring #0<br>1: RX Ring #1 | 0x0 |
| 1 | RW | PRI1_RING | Priority 1 to RX Ring#<br>0: RX Ring #0<br>1: RX Ring #1 | 0x0 |
| 0 | RW | PRI0_RING | Priority 0 to RX Ring#<br>0: RX Ring #0<br>1: RX Ring #1 | 0x0 |

## SDM\_TRING: Switch DMA TX Ring Register(offset: 0x0008)

| Bits  | Type | Name         | Description                                                                                                                                                                                                                             | Initial value |
|-------|------|--------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:28 | RW   | RING3_WAN_FC | Pause TX Ring 3 by WAN Port<br>TX Ring# will be paused when the corresponding switch egress queue on WAN port is congested.<br>Bit.3: WAN port Queue#3<br>Bit.2: WAN port Queue#2<br>Bit.1: WAN port Queue#1<br>Bit.0: WAN port Queue#0 | 0x0           |
| 27:24 | RW   | RING2_WAN_FC | Pause TX Ring 2 by WAN Port<br>TX Ring# will be paused when the corresponding switch egress queue on WAN port is congested.<br>Bit.3: WAN port Queue#3<br>Bit.2: WAN port Queue#2<br>Bit.1: WAN port Queue#1<br>Bit.0: WAN port Queue#0 | 0x0           |
| 23:20 | RW   | RING1_WAN_FC | Pause TX Ring 1 by WAN Port<br>TX Ring# will be paused when the corresponding switch egress queue on WAN port is congested.<br>Bit.3: WAN port Queue#3<br>Bit.2: WAN port Queue#2<br>Bit.1: WAN port Queue#1<br>Bit.0: WAN port Queue#0 | 0x0           |
| 19:16 | RW   | RING0_WAN_FC | Pause TX Ring 0 by WAN Port<br>TX Ring# will be paused when the corresponding switch egress queue on WAN port is congested.<br>Bit.3: WAN port Queue#3<br>Bit.2: WAN port Queue#2<br>Bit.1: WAN port Queue#1<br>Bit.0: WAN port Queue#0 | 0x0           |
| 15:12 | RW   | RING3_LAN_FC | Pause TX Ring 3 by LAN Port<br>TX Ring# will be paused when the corresponding switch egress queue on LAN port is congested.<br>Bit.3: LAN port Queue#3<br>Bit.2: LAN port Queue#2                                                       | 0x0           |

|      |    |              |                                                                                                                                                                                                                                         |     |
|------|----|--------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|
|      |    |              | Bit.1: LAN port Queue#1<br>Bit.0: LAN port Queue#0                                                                                                                                                                                      |     |
| 11:8 | RW | RING2_LAN_FC | Pause TX Ring 2 by LAN Port<br>TX Ring# will be paused when the corresponding switch egress queue on LAN port is congested.<br>Bit.3: LAN port Queue#3<br>Bit.2: LAN port Queue#2<br>Bit.1: LAN port Queue#1<br>Bit.0: LAN port Queue#0 | 0x0 |
| 7:4  | RW | RING1_LAN_FC | Pause TX Ring 1 by LAN Port<br>TX Ring# will be paused when the corresponding switch egress queue on LAN port is congested.<br>Bit.3: LAN port Queue#3<br>Bit.2: LAN port Queue#2<br>Bit.1: LAN port Queue#1<br>Bit.0: LAN port Queue#0 | 0x0 |
| 3:0  | RW | RING0_LAN_FC | Pause TX Ring 0 by LAN Port<br>TX Ring# will be paused when the corresponding switch egress queue on LAN port is congested.<br>Bit.3: LAN port Queue#3<br>Bit.2: LAN port Queue#2<br>Bit.1: LAN port Queue#1<br>Bit.0: LAN port Queue#0 | 0x0 |

SDM\_MAC\_ADRL: Switch MAC Address LSB Register(offset: 0x000c)

| Bits | Type | Name     | Description                | Initial value |
|------|------|----------|----------------------------|---------------|
| 31:0 | RW   | MY_MAC_L | MAC Address Bit.31 – Bit.0 | 0x0           |

SDM\_MAC\_ADRH: Switch MAC Address MSB Register(offset: 0x0010)

| Bits  | Type | Name     | Description                 | Initial value |
|-------|------|----------|-----------------------------|---------------|
| 31:16 | -    | RES      | Reserved                    | -             |
| 15:0  | RW   | MY_MAC_H | MAC Address Bit.47 – Bit.32 | 0x0           |

SDM\_TPCNT: Switch DMA TX Packet Counter(offset: 0x0100)

| Bits | Type | Name    | Description                                                           | Initial value |
|------|------|---------|-----------------------------------------------------------------------|---------------|
| 31:0 | RC   | TX_PCNT | Transmit Packet Count<br>Frame Engine to Switch Transmit Packet Count | 0x0           |

SDM\_TBCNT: Switch DMA TX Byte Counter(offset: 0x0104)

| Bits | Type | Name    | Description                                                       | Initial value |
|------|------|---------|-------------------------------------------------------------------|---------------|
| 31:0 | RC   | TX_BCNT | Transmit Byte Count<br>Frame Engine to Switch Transmit Byte Count | 0x0           |

SDM\_RPCNT: Switch DMA RX Packet Counter(offset: 0x0108)

| Bits | Type | Name | Description | Initial value |
|------|------|------|-------------|---------------|
|------|------|------|-------------|---------------|

|      |    |         |                                                                     |     |
|------|----|---------|---------------------------------------------------------------------|-----|
| 31:0 | RC | RX_PCNT | Receive Packet Count<br>Switch to Frame Engine Receive Packet Count | 0x0 |
|------|----|---------|---------------------------------------------------------------------|-----|

SDM\_RBCNT: Switch DMA RX Byte Counter(offset: 0x010c)

| Bits | Type | Name    | Description                                                     | Initial value |
|------|------|---------|-----------------------------------------------------------------|---------------|
| 31:0 | RC   | RX_BCNT | Receive Byte Count<br>Switch to Frame Engine Receive Byte Count | 0x0           |

SDM\_CS\_ERR: Switch DMA RX Checksum Error Counter(offset: 0x0110)

| Bits | Type | Name    | Description                                                              | Initial value |
|------|------|---------|--------------------------------------------------------------------------|---------------|
| 31:0 | RC   | TX_PCNT | Receive Checksum Error Count<br>Frame EngineReceive Checksum Error Count | 0x0           |

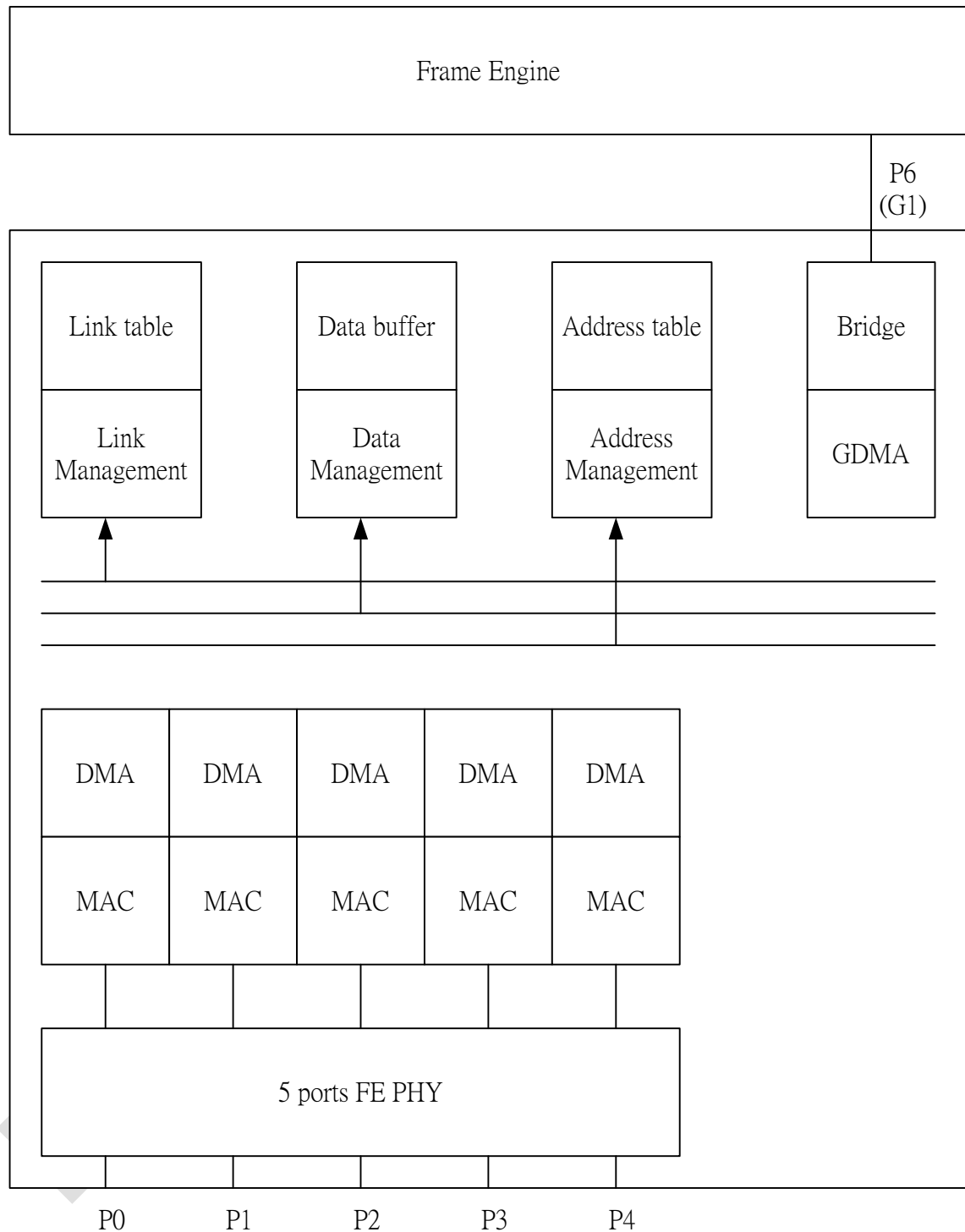
### 3.20 Ethernet Switch

#### 3.20.1 Features

- Support IEEE 802.3 full duplex flow control
- 5 10/100Mbps PHY
- Support Spanning Tree port states
- Support 1K-MAC address table with direct or XOR hash
- QoS
  - Four priorities queues per port
  - Packet classification based on incoming port, IEEE 802.1p or IP ToS/DSCP
  - Strict-Priority Queue (PQ) and Weighted Round Robin (WRR)
- VLAN
  - Port Base VLAN
  - Double VLAN tagging
  - 802.1q tag VLAN
  - 16 VIDs
- MAC address table read and write-able
- MAC security – Locking a MAC address to an incoming port
- MAC clone support – hash with VID
- IGMP and MLD support
- Per-Port Broadcast storm prevention

[Note] : RT5350 doesn't have port5 Giga MAC on chip. The corresponding port 5 registers are reserved and invalid.



**3.20.2 Block Diagram**

**Fig. 3-18-1 Ethernet Switch Block Diagram**

Draft

### 3.20.3 Frame Classification

| FTAG      | DA                                          | Type  | IPv4/IPv6 Protocol                 | Description                                         |
|-----------|---------------------------------------------|-------|------------------------------------|-----------------------------------------------------|
| BC        | FF-FF-FF-FF-FF-FF                           | -     | -                                  | Broadcast Frames                                    |
| MC        | Bit.40=1'b1                                 | -     | -                                  | Multicast Frames                                    |
| IGMP      | 01-00-5E-xx-xx-xx                           | 08-00 | 0x02                               | IGMP Message Packet                                 |
| IP_MULT   | 01-00-5E-xx-xx-xx                           | -     | -                                  | IP Multicast Frames                                 |
| MLD       | 33-33-xx-xx-xx-xx                           | 86-DD | 0x00 (Hop_by_Hop)<br>0x3A (ICMPv6) | MLD/ICMPv6 Message Packet                           |
| IPV6_MULT | 33-33-xx-xx-xx-xx                           | -     | -                                  | IPv6 Multicast Frames                               |
| PAUSE     | -                                           | 88-08 | -                                  | Discarded                                           |
|           | 01-80-C2-00-00-01<br>Or<br>Unicast DA       | 88-08 | Followed by 00-01                  | MAC Control Pause Frame (< 1518 bytes)<br>Discarded |
| RMC       | 01-80-C2-00-00-00                           | -     | -                                  | BPDU                                                |
|           | 01-80-C2-00-00-02<br>~<br>01-80-c2-00-00-xx | -     | -                                  | Reserved Group/Multicast Frames                     |

Fig. 3-18-2 Reserved Multicast Address Frames

### 3.20.4 Register Description(base: 0x1011\_0000)

Note : In RT5350, the registers related to P5 (port 5) are not applicable. Please keep them as default settings  
ISR: Interrupt Status Register(offset: 0x0000)

| Bits | Type | Name                  | Description                                                                                                                                                                                                                  | Initial value |
|------|------|-----------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31   | RO   | PKT_CNT_              | <b>This bit indicates that any status change of the packet counter interrupt status(PCIS offset: 0x14C). To clear this bit, write one to PCRI register.</b>                                                                  | 0x0           |
| 30   | -    | -                     | Reserved                                                                                                                                                                                                                     | 0x0           |
| 29   | RW   | WATCHDOG1_TMR_EXPIRED | P5 no transmit packet alert.<br>This bit indicating that P5 don't transmit packet for 3 seconds when P5 need to transmit packet. Write one clear.<br>(Note: This feature is only valid when port 5 Giga MAC is implemented.) | 0x0           |
| 28   | RW   | WATCHDOG0_TMR_EXPIRED | Abnormal Alert<br>This bit indicating that global queue block counts is less than buf_starvation_th for 3 seconds. Write one clear.                                                                                          | 0x0           |
| 27   | RW   | HAS_INTRUDER          | Intruder Alert<br>This bit indicating that an unsecured packet is coming into a secured port. Write one clear.                                                                                                               | 0x0           |
| 26   | RW   | PORT_ST_CHG           | Port status change<br>Any port from link status change. Write one clear.                                                                                                                                                     | 0x0           |
| 25   | RW   | BC_STORM              | BC storm<br>The device is undergoing broadcast storm. Write one clear.                                                                                                                                                       | 0x0           |
| 24   | RW   | MUST_DROP_LAN         | Queue exhausted<br>The global queue is used up and all packets are dropped. Write one clear.                                                                                                                                 | 0x0           |

|       |    |                 |                                                                                                                   |     |
|-------|----|-----------------|-------------------------------------------------------------------------------------------------------------------|-----|
| 23    | RW | GLOBAL_QUE_FULL | Global Queue Full. Write one clear.                                                                               | 0x0 |
| 22:21 | -  | -               | Reserved                                                                                                          | -   |
| 20    | RW | LAN_QUE_FULL[6] | Port6 out queue full. Write one clear.                                                                            | 0x0 |
| 19    | RW | LAN_QUE_FULL[5] | Port5 out queue full. Write one clear.<br>(Note: This feature is only valid when port 5 Giga MAC is implemented.) | 0x0 |
| 18    | RW | LAN_QUE_FULL[4] | Port4 out queue full. Write one clear.                                                                            | 0x0 |
| 17    | RW | LAN_QUE_FULL[3] | Port3 out queue full. Write one clear.                                                                            | 0x0 |
| 16    | RW | LAN_QUE_FULL[2] | Port2 out queue full. Write one clear.                                                                            | 0x0 |
| 15    | RW | LAN_QUE_FULL[1] | Port1 out queue full. Write one clear.                                                                            | 0x0 |
| 14    | RW | LAN_QUE_FULL[0] | Port0 out queue full. Write one clear.                                                                            | 0x0 |
| 13:0  | -  | -               | Reserved                                                                                                          | 0x0 |

IMR: Interrupt Mask Register (offset: 0x0004)

| Bits  | Type | Name            | Description                                                                                                                                                                                                 | Initial value |
|-------|------|-----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31    | RW   | PKT_CNT_MASK_31 | Packet count mask of 31 bits                                                                                                                                                                                | 0x1           |
| 30    | -    | -               | Reserved                                                                                                                                                                                                    | -             |
| 29    | RW   | SW_INT_MASK_29  | P5 no transmit packet alert.<br>This bit indicating that P5 don't transmit packet for 3 seconds when P5 need to transmit packet.<br>(Note: This feature is only valid when port 5 Giga MAC is implemented.) | 0x1           |
| 28    | RW   | SW_INT_MASK_28  | Abnormal Alert<br>This bit indicating that global queue block counts is less than buf_starvation_th for 3 seconds.                                                                                          | 0x1           |
| 27    | RW   | SW_INT_MASK_27  | Intruder Alert<br>This bit indicating that an unsecured packet is coming into a secured port.                                                                                                               | 0x1           |
| 26    | RW   | SW_INT_MASK_26  | Port status change<br>Any port from link status change                                                                                                                                                      | 0x1           |
| 25    | RW   | SW_INT_MASK_25  | BC storm<br>The device is undergoing broadcast storm                                                                                                                                                        | 0x1           |
| 24    | RW   | SW_INT_MASK_24  | Queue exhausted<br>The global queue is used up and all packets are dropped                                                                                                                                  | 0x1           |
| 23    | RW   | SW_INT_MASK_23  | Shared queue full                                                                                                                                                                                           | 0x1           |
| 22:21 | -    | -               | Reserved                                                                                                                                                                                                    | -             |
| 20    | RW   | SW_INT_MASK_20  | port6 queue full                                                                                                                                                                                            | 0x1           |
| 19    | RW   | SW_INT_MASK_19  | port5 queue full<br>(Note: This feature is only valid when port 5 Giga MAC is implemented)                                                                                                                  | 0x1           |
| 18    | RW   | SW_INT_MASK_18  | port4 queue full                                                                                                                                                                                            | 0x1           |
| 17    | RW   | SW_INT_MASK_17  | port3 queue full                                                                                                                                                                                            | 0x1           |
| 16    | RW   | SW_INT_MASK_16  | port2 queue full                                                                                                                                                                                            | 0x1           |
| 15    | RW   | SW_INT_MASK_15  | port1 queue full                                                                                                                                                                                            | 0x1           |
| 14    | RW   | SW_INT_MASK_14  | port0 queue full                                                                                                                                                                                            | 0x1           |
| 13:0  | -    | -               | Reserved                                                                                                                                                                                                    | -             |

FCT0: Flow Control Threshold 0 (offset: 0x0008)

| Bits | Type | Name | Description | Initial value |
|------|------|------|-------------|---------------|
|------|------|------|-------------|---------------|

|       |    |             |                                                                                                                                                  |      |
|-------|----|-------------|--------------------------------------------------------------------------------------------------------------------------------------------------|------|
| 31:24 | RW | FC_RLS_TH   | Flow Control Release Threshold<br>Flow control will be disabled when the global queue block counts is greater than the release threshold         | 0xFF |
| 23:16 | RW | FC_SET_TH   | Flow Control Set Threshold<br>Flow control will be enabled when the global queue block counts is less than the set threshold                     | 0xC8 |
| 15:8  | RW | DROP_RLS_TH | <b>Drop Release Threshold</b><br>Switch will stop dropping packets when the global queue block counts is greater than the drop-release threshold | 0x6E |
| 7:0   | RW | DROP_SET_TH | <b>Drop Set Threshold</b><br>Switch will start dropping packets when the global queue block counts is less than the drop-set threshold.          | 0x5A |

**FCT1: Flow Control Threshold 1 (offset: 0x000c)**

| Bits | Type | Name    | Description                                                                                                                                                                                                                                                          | Initial value |
|------|------|---------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:8 | -    | -       | Reserved                                                                                                                                                                                                                                                             | -             |
| 7:0  | RW   | PORT_TH | Per Port Output Threshold<br>When the global queue reaches the flow control or drop threshold on register FCT0, per port output threshold will be checked to enable flow-control or packet-drop depending on per queue minimum reserved blocks of the register PFC2. | 0x14          |

**PFC0: Priority flow control – 0 (offset: 0x0010)**

| Bits  | Type | Name        | Description                                                                                                                                                                                     | Initial value |
|-------|------|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:28 | -    | -           | Reserved                                                                                                                                                                                        | -             |
| 27:24 | RW   | MTCC_LMT    | MTCC LIMIT<br>The maximum Back-off count limit to drop excessive collision packets.                                                                                                             | 0xF           |
| 23    | -    | -           | Reserved                                                                                                                                                                                        | -             |
| 22:16 | RW   | TURN_OFF_FC | Turn off FC When Receiving High Packet<br>Auto-turn-off FC when the programmed ports receive one of the highest priority packet.<br><u>0: disable</u><br><u>1: enable</u>                       | 0x0           |
| 15:12 | RW   | VO_NUM      | The proportional number of WRR for Voice Queue<br>After transmit exactly the number of packets then proceed to next queue. If equal to 0, only this queue is forced to the strict priority mode | 0x0           |
| 11:8  | RW   | CL_NUM      | The proportional number of WRR for Control-Load Queue<br>After transmit exactly the number of packet then proceed to next queue.                                                                | 0x0           |
| 7:4   | RW   | BE_NUM      | The proportional number of WRR for Best-Effort Queue<br>After transmit exactly the number of packet then proceed to next queue.                                                                 | 0x0           |
| 3:0   | RW   | BK_NUM      | The proportional number of WRR for Background Queue<br>After transmit exactly the number of packet then proceed to next queue.                                                                  | 0x0           |

**PFC1: Priority Flow control –1 (offset: 0x0014)**

| Bits | Type | Name          | Description                                                                                                               | Initial value |
|------|------|---------------|---------------------------------------------------------------------------------------------------------------------------|---------------|
| 31   | RW   | CPU_USE_Q1_EN | CPU Port only use q1 enable<br>0: default priority resolution<br>1: packets forwarded to CPU port uses Best-Effort Queue. | 0x0           |

|       |    |                 |                                                                                                                                                                                        |     |
|-------|----|-----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|
| 30:24 | RW | EN_TOS[7:0]     | Port6 ~ port0 TOS_en.<br>Check TOS field of IP packets for priority resolution.<br>0: disable<br>1 :enable<br>(Note: Port5 function is only valid when port 5 Giga MAC is implemented) | 0x0 |
| 23    | RW | IGMP_to_CPU     | IGMP forward to CPU enable<br>1'b0 : IGMP message will be flooded to all ports<br>1'b1 : IGMP message will be forwarded to CPU port only.                                              | 0x0 |
| 22:16 | RW | EN_VLAN         | Enable per port VLAN-tag VID membership and priority tag check.<br>0: disable.<br>1: enable<br>(Note: Port5 function is only valid when port 5 Giga MAC is implemented)                | 0x0 |
| 15    | RW | PRIORITY_OPTION | Priority Resolution Option<br>0 : 802.1p → TOS → Per port<br>1 : TOS → 802.1p → Per port                                                                                               | 0x0 |
| 14    | -  | -               | Reserved                                                                                                                                                                               | -   |
| 13:12 | RW | PORT_PRI6       | Port priority<br>By setting this register to assign per port's default priority queue.                                                                                                 | 0x1 |
| 11:10 | RW | PORT_PRI5       | Port priority<br>By setting this register to assign per port's default priority queue.<br>(Note: This feature is only valid when port 5 Giga MAC is implemented)                       | 0x1 |
| 9:8   | RW | PORT_PRI4       | Port priority<br>By setting this register to assign per port's default priority queue.                                                                                                 | 0x1 |
| 7:6   | RW | PORT_PRI3       | Port priority<br>By setting this register to assign per port's default priority queue.                                                                                                 | 0x1 |
| 5:4   | RW | PORT_PRI2       | Port priority<br>By setting this register to assign per port's default priority queue.                                                                                                 | 0x1 |
| 3:2   | RW | PORT_PRI1       | Port priority<br>By setting this register to assign per port's default priority queue.                                                                                                 | 0x1 |
| 1:0   | RW | PORT_PRI0       | Port priority<br>By setting this register to assign per port's default priority queue.                                                                                                 | 0x1 |

**PFC2: Priority flow control –2 (offset: 0x0018)**

| Bits  | Type | Name      | Description                                                                                                                                                                                                                                                                      | Initial value |
|-------|------|-----------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:24 | RW   | PRI_TH_VO | Voice Threshold – Highest Priority<br>The minimum reserved packet block count which output queue can store when the flow-control/drop threshold of registers FTC0 and FCT1 is reached. If the queued blocks exceed the threshold, the incoming packet will be paused or dropped. | 0x3           |

|       |    |           |                                                                                                                                                                                                                                                                                      |     |
|-------|----|-----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|
| 23:16 | RW | PRI_TH_CL | Control Load Threshold<br>The minimum reserved packet block count which outout queue can store when the flow-control/drop threshold of registers FTC0 and FCT1 is reached. If the queued blocks exceed the threshold, the incoming packet will be paused or dropped.                 | 0x3 |
| 15:8  | RW | PRI_TH_BE | Best Effort threshold<br>The minimum reserved packet block count which outout queue can store when the flow-control/drop threshold of registers FTC0 and FCT1 is reached. If the queued blocks exceed the threshold, the incoming packet will be paused or dropped.                  | 0x3 |
| 7:0   | RW | PRI_TH_BK | Background Threshold – Lowest Priority<br>The minimum reserved packet block count which outout queue can store when the flow-control/drop threshold of registers FTC0 and FCT1 is reached. If the queued blocks exceed the threshold, the incoming packet will be paused or dropped. | 0x3 |

**GQS0: Global Queue Status – 0 (offset: 0x001c)**

| Bits  | Type | Name      | Description                                                                                                | Initial value |
|-------|------|-----------|------------------------------------------------------------------------------------------------------------|---------------|
| 31:30 | RW   | PRI7_QUE  | Queue mapping for Priority Tag #7                                                                          | 0x3           |
| 29:28 | RW   | PRI6_QUE  | Queue mapping for Priority Tag #6                                                                          | 0x3           |
| 27:26 | RW   | PRI5_QUE  | Queue mapping for Priority Tag #5                                                                          | 0x2           |
| 25:24 | RW   | PRI4_QUE  | Queue mapping for Priority Tag #4                                                                          | 0x2           |
| 23:22 | RW   | PRI3_QUE  | Queue mapping for Priority Tag #3                                                                          | 0x1           |
| 21:20 | RW   | PRI2_QUE  | Queue mapping for Priority Tag #2                                                                          | 0x0           |
| 19:18 | RW   | PRI1_QUE  | Queue mapping for Priority Tag #1                                                                          | 0x0           |
| 17:16 | RW   | PRI0_QUE  | Queue mapping for Priority Tag #0                                                                          | 0x1           |
| 15:9  | -    | -         | Reserved                                                                                                   | 0x0           |
| 8:0   | RO   | EMPTY_CNT | Global Queue Block Counts<br>This field indicates the number of block count left in the global free queue. | 0x16e         |

**GQS1: Global Queue Status – 1 (offset: 0x0020)**

| Bits  | Type | Name           | Description                                                          | Initial value |
|-------|------|----------------|----------------------------------------------------------------------|---------------|
| 31    | -    | -              | Reserved                                                             | -             |
| 30:24 | RO   | OUTQUE_FULL_VO | Congested Voice Queue<br>The corresponding queue is congested        | 0x0           |
| 24    | -    | -              | Reserved                                                             | -             |
| 23:16 | RO   | OUTQUE_FULL_CL | Congested Control Load Queue<br>The corresponding queue is congested | 0x0           |
| 15    | -    | -              | Reserved                                                             | -             |
| 14:8  | RO   | OUTQUE_FULL_BE | Congested Best Effort Queue<br>The corresponding queue is congested  | 0x0           |
| 7     | -    | -              | Reserved                                                             | -             |
| 6:0   | RO   | OUTQUE_FULL_BK | Congested Background Queue<br>The corresponding queue is congested   | 0x0           |

**ATS: Address Table Search (offset: 0x0024)**

| Bits | Type | Name         | Description                                                                            | Initial value |
|------|------|--------------|----------------------------------------------------------------------------------------|---------------|
| 31:3 | -    | -            | Reserved                                                                               | 0x0           |
| 2    | RS   | AT_LKUP_IDLE | Address Lookup Idle<br>This field indicates that Adress Table engine is in IDLE state. | 0x0           |

|   |    |                   |                                                |     |
|---|----|-------------------|------------------------------------------------|-----|
| 1 | RW | SEARCH_NXT_ADDR   | Search For The Next Address (Self_Clear)       | 0x0 |
| 0 | RW | BEGIN_SEARCH_ADDR | Start Searching The Address Table (Self_Clear) | 0x0 |

**ATS0: Address Table Status 0 (offset: 0x0028)**

| Bits  | Type | Name         | Description                                 | Initial value |
|-------|------|--------------|---------------------------------------------|---------------|
| 31:22 | RO   | HASH_ADD_LU  | Address table lookup address                | 0x0           |
| 21:19 | -    | -            | Reserved                                    | -             |
| 18:12 | RO   | R_PORT_MAP   | Port map<br>The MAC existing in the bit =1. | 0x0           |
| 11    | -    | -            | Reserved                                    | -             |
| 10:7  | RO   | R_VID        | VLAN index                                  | 0x0           |
| 6:4   | RO   | R_AGE_FIELD  | Aging field                                 | 0x0           |
| 3     | -    | -            | Reserved                                    | -             |
| 2     | RO   | R_MC_INGRESS | MC Ingress                                  | 0x0           |
| 1     | RO   | AT_TABLE_END | Search to the end of address table          | 0x0           |
| 0     | RO   | SEARCH_RDY   | Data is ready (read clear)                  | 0x0           |

**ATS1: Address Table Status 1 (offset: 0x002c)**

| Bits  | Type | Name        | Description             | Initial value |
|-------|------|-------------|-------------------------|---------------|
| 31:16 | -    | -           | Reserved                | -             |
| 15:0  | RO   | MAC_AD_SER0 | Read MAC address [15:0] | 0x0           |

**ATS2: Address Table Status 2 (offset: 0x0030)**

| Bits | Type | Name        | Description              | Initial value |
|------|------|-------------|--------------------------|---------------|
| 31:0 | RO   | MAC_AD_SER1 | Read MAC address [47:16] | 0x0           |

**WMAD0: WT\_MAC\_AD0 (offset: 0x0034)**

| Bits  | Type | Name         | Description                                                                                                                             | Initial value |
|-------|------|--------------|-----------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:22 | RO   | HASH_ADD_CFG | Address table configuration address                                                                                                     | 0x0           |
| 21:19 | -    | -            | Reserved                                                                                                                                | -             |
| 19    | RO   | AT_CFG_IDLE  | Address table configuration SM idle                                                                                                     | 0x1           |
| 18:12 | RW   | W_PORT_MAP   | Write Port Bit-map                                                                                                                      | 0x0           |
| 11    | -    | -            | Reserved                                                                                                                                | -             |
| 10:7  | RW   | W_INDEX      | Write VLAN Index<br>0: VLAN 0<br>~<br>15: VLAN 15                                                                                       | 0x0           |
| 6:4   | RW   | W_AGE_FIELD  | Write aging field,<br>111b : static address,<br>001b ~110b: the entry is valid and will be aged out<br>000b : default, entry is invalid | 0x0           |
| 3     | RW   | -SA_FILTER   | SA_FILTER<br>0: default<br>1: the corresponding packet will be dropped when the SA is matched.                                          | 0x0           |
| 2     | RW   | W_MC_INGRESS | Write Mc_Ingress Bit                                                                                                                    | 0x0           |
| 1     | RO   | W_MAC_DONE   | MAC Write Done<br>0: default<br>1: MAC address write OK, (read_clear)                                                                   | 0x0           |
| 0     | RW   | W_MAC_CMD    | MAC Address Write Command<br>0: default<br>1: the MAC write data is ready and write to MAC table now, self_clear                        | 0x0           |

**WMAD1: WT\_MAC\_AD1 (offset: 0x0038)**

| Bits  | Type | Name       | Description              | Initial value |
|-------|------|------------|--------------------------|---------------|
| 31:16 | -    | -          | Reserved                 | 0x0           |
| 15:0  | RW   | W_MAC_15_0 | Write MAC address [15:0] | 0x0           |

**WMAD2: WT\_MAC\_AD2 (offset: 0x003c)**

| Bits | Type | Name        | Description               | Initial value |
|------|------|-------------|---------------------------|---------------|
| 31:0 | RW   | W_MAC_47_16 | Write MAC address [47:16] | 0x0           |

**PVIDC0: PVID Configuration 0 (offset: 0x0040)**

| Bits  | Type | Name    | Description        | Initial value |
|-------|------|---------|--------------------|---------------|
| 31:24 | -    | -       | Reserved           | -             |
| 23:12 | RW   | P1_PVID | Port1 PVID setting | 0x1           |
| 11:0  | RW   | P0_PVID | Port0 PVID setting | 0x1           |

**PVIDC1: PVID Configuration 1 (offset: 0x0044)**

| Bits  | Type | Name    | Description        | Initial value |
|-------|------|---------|--------------------|---------------|
| 31:24 | -    | -       | Reserved           | -             |
| 23:12 | RW   | P3_PVID | Port3 PVID setting | 0x1           |
| 11:0  | RW   | P2_PVID | Port2 PVID setting | 0x1           |

**PVIDC2: PVID Configuration 2 (offset: 0x0048)**

| Bits  | Type | Name    | Description                                                                                  | Initial value |
|-------|------|---------|----------------------------------------------------------------------------------------------|---------------|
| 31:24 | -    | -       | Reserved                                                                                     | -             |
| 23:12 | RW   | P5_PVID | Port5 PVID setting<br>(Note: This feature is only valid when port 5 Giga MAC is implemented) | 0x1           |
| 11:0  | RW   | P4_PVID | Port4 PVID setting                                                                           | 0x1           |

**PVIDC3: PVID Configuration 3 (offset: 0x004c)**

| Bits  | Type | Name      | Description                                          | Initial value |
|-------|------|-----------|------------------------------------------------------|---------------|
| 31    | -    | -         | Reserved                                             | 0x0           |
| 30:28 | RW   | QUE3_PRIT | Priority Tag Egress Mapping for Voice Queue#3        | 0x7           |
| 27    | -    | -         | Reserved                                             | 0x0           |
| 26:24 | RW   | QUE2_PRIT | Priority Tag Egress Mapping for Control Load Queue#2 | 0x5           |
| 23    | -    | -         | Reserved                                             | 0x0           |
| 22:20 | RW   | QUE1_PRIT | Priority Tag Egress Mapping for Best Effort Queue#1  | 0x0           |
| 19    | -    | -         | Reserved                                             | 0x0           |
| 18:16 | RW   | QUE0_PRIT | Priority Tag Egress Mapping for Background Queue#0   | 0x2           |
| 15:12 | -    | -         | Reserved                                             | 0x0           |
| 11:0  | RW   | P6_PVID   | Port6 PVID setting                                   | 0x1           |

**VLANI0: VLAN Identifier 0 (offset: 0x0050)**

| Bits  | Type | Name | Description                      | Initial value |
|-------|------|------|----------------------------------|---------------|
| 31:24 | -    | -    | Reserved                         | -             |
| 23:12 | RW   | VID1 | VLAN field Identifier for VLAN 1 | 0x2           |
| 11:0  | RW   | VID0 | VLAN field Identifier for VLAN 0 | 0x1           |

**VLANI1: VLAN Identifier 1 (offset: 0x0054)**

| Bits  | Type | Name | Description                      | Initial value |
|-------|------|------|----------------------------------|---------------|
| 31:24 | -    | -    | Reserved                         | -             |
| 23:12 | RW   | VID3 | VLAN field Identifier for VLAN 3 | 0x4           |
| 11:0  | RW   | VID2 | VLAN field Identifier for VLAN 2 | 0x3           |

**VLANI2: VLAN Identifier 2 (offset: 0x0058)**

| Bits  | Type | Name | Description                      | Initial value |
|-------|------|------|----------------------------------|---------------|
| 31:24 | -    | -    | Reserved                         | -             |
| 23:12 | RW   | VID5 | VLAN field Identifier for VLAN 5 | 0x6           |



|      |    |      |                                  |     |
|------|----|------|----------------------------------|-----|
| 11:0 | RW | VID4 | VLAN field Identifier for VLAN 4 | 0x5 |
|------|----|------|----------------------------------|-----|

**VLANI3: VLAN Identifier 3 (offset: 0x005c)**

| Bits  | Type | Name | Description                      | Initial value |
|-------|------|------|----------------------------------|---------------|
| 31:24 | -    | -    | Reserved                         | -             |
| 23:12 | RW   | VID7 | VLAN field Identifier for VLAN 7 | 0x8           |
| 11:0  | RW   | VID6 | VLAN field Identifier for VLAN 6 | 0x7           |

**VLANI4: VLAN Identifier 4 (offset: 0x0060)**

| Bits  | Type | Name | Description                      | Initial value |
|-------|------|------|----------------------------------|---------------|
| 31:24 | -    | -    | Reserved                         | -             |
| 23:12 | RW   | VID9 | VLAN field Identifier for VLAN 9 | 0xA           |
| 11:0  | RW   | VID8 | VLAN field Identifier for VLAN 8 | 0x9           |

**VLANI5: VLAN Identifier 5 (offset: 0x0064)**

| Bits  | Type | Name  | Description                       | Initial value |
|-------|------|-------|-----------------------------------|---------------|
| 31:24 | -    | -     | Reserved                          | -             |
| 23:12 | RW   | VID11 | VLAN field Identifier for VLAN 11 | 0xC           |
| 11:0  | RW   | VID10 | VLAN field Identifier for VLAN 10 | 0xB           |

**VLANI6: VLAN Identifier 6 (offset: 0x0068)**

| Bits  | Type | Name  | Description                       | Initial value |
|-------|------|-------|-----------------------------------|---------------|
| 31:24 | -    | -     | Reserved                          | 0x0           |
| 23:12 | RW   | vid13 | VLAN field Identifier for VLAN 13 | 0xE           |
| 11:0  | RW   | vid12 | VLAN field Identifier for VLAN 12 | 0xD           |

**VLANI7: VLAN Identifier 7 (offset: 0x006c)**

| Bits  | Type | Name  | Description                 | Initial value |
|-------|------|-------|-----------------------------|---------------|
| 31:24 | -    | -     | Reserved                    | 0x0           |
| 23:12 | RW   | VID15 | VLAN Identifier for VLAN 15 | 0x10          |
| 11:0  | RW   | VID14 | VLAN Identifier for VLAN 14 | 0xF           |

**VMSC0: VLAN Member Port Configuration 0 (offset: 0x0070)**

| Bits  | Type | Name          | Description        | Initial value |
|-------|------|---------------|--------------------|---------------|
| 30:24 | RW   | VLAN_MEMSET_3 | VLAN 3 member port | 0x7F          |
| 22:16 | RW   | VLAN_MEMSET_2 | VLAN 2 member port | 0x7F          |
| 15:8  | RW   | VLAN_MEMSET_1 | VLAN 1 member port | 0x7F          |
| 7:0   | RW   | VLAN_MEMSET_0 | VLAN 0 member port | 0x7F          |

**VMSC1: VLAN Member Port Configuration 1 (offset: 0x0074)**

| Bits  | Type | Name          | Description        | Initial value |
|-------|------|---------------|--------------------|---------------|
| 30:24 | RW   | VLAN_MEMSET_7 | VLAN 7 member port | 0x7F          |
| 22:16 | RW   | VLAN_MEMSET_6 | VLAN 6 member port | 0x7F          |
| 15:8  | RW   | VLAN_MEMSET_5 | VLAN 5 member port | 0x7F          |
| 7:0   | RW   | VLAN_MEMSET_4 | VLAN 4 member port | 0x7F          |

**VMSC2: VLAN Member Port Configuration 2 (offset: 0x0078)**

| Bits  | Type | Name           | Description         | Initial value |
|-------|------|----------------|---------------------|---------------|
| 30:24 | RW   | VLAN_MEMSET_11 | VLAN 11 member port | 0x7F          |
| 22:16 | RW   | VLAN_MEMSET_10 | VLAN 10 member port | 0x7F          |
| 15:8  | RW   | VLAN_MEMSET_9  | VLAN 9 member port  | 0x7F          |
| 7:0   | RW   | VLAN_MEMSET_8  | VLAN 8 member port  | 0x7F          |

**VMSC3: VLAN Member Port Configuration 3 (offset: 0x007c)**

| Bits  | Type | Name           | Description         | Initial value |
|-------|------|----------------|---------------------|---------------|
| 30:24 | RW   | VLAN_MEMSET_15 | VLAN 15 member port | 0x7F          |
| 22:16 | RW   | VLAN_MEMSET_14 | VLAN 14 member port | 0x7F          |
| 15:8  | RW   | VLAN_MEMSET_13 | VLAN 13 member port | 0x7F          |
| 7:0   | RW   | VLAN_MEMSET_12 | VLAN 12 member port | 0x7F          |

POA: Port Ability (offset: 0x0080)

| Bits  | Type | Name    | Description                                                                                                                                                                                                                                                                                            | Initial value |
|-------|------|---------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31    | RO   | G1_LINK | Port 6 Link Status<br>1: Link up<br>0: Link down                                                                                                                                                                                                                                                       | 0x0           |
| 30    | RO   | G0_LINK | Port 5 Link Status<br>1: Link up<br>0: Link down<br>(Note: This feature is only valid when port 5 Giga MAC is implemented)                                                                                                                                                                             | 0x0           |
| 29:25 | RO   | LINK    | Port 4 ~ port 0 Link Status<br>1: Link up<br>0: Link down                                                                                                                                                                                                                                              | 0x0           |
| 24:23 | RO   | G1_XFC  | Flow Control Status of Port 6<br>The flow control capability status bit after Auto-negotiation or force mode.<br>1xb: full duplex and tx flow control ON<br>x1b: full duplex and rx flow control ON<br>00b: flow control off                                                                           | 0x0           |
| 22:21 | RO   | G0_XFC  | Flow Control Status of Port 5<br>The flow control capability status bit after Auto-negotiation or force mode.<br>1xb: full duplex and tx flow control ON<br>x1b: full duplex and rx flow control ON<br>00b: flow control off<br>(Note: This feature is only valid when port 5 Giga MAC is implemented) | 0x0           |
| 20:16 | RO   | XFC     | Flow Control Status of port 0 ~ 4<br>The flow control capability status bit after Auto-negotiation or force mode.<br>0: flow control off<br>1 : full duplex and 802.3x flow control ON (after AN or forced)                                                                                            | 0x0           |
| 15:9  | RO   | DUPLEX  | Port6 ~ port0 Duplex Mode<br>0: half duplex<br>1: full duplex<br>(Note: Port5 function is only valid when port 5 Giga MAC is implemented)                                                                                                                                                              | 0x0           |
| 8:7   | RO   | G1_SPD  | MII port 6 Speed Mode<br>10: 1GHz, 01: 100M, 00: 10M                                                                                                                                                                                                                                                   | 0x0           |
| 6:5   | RO   | G0_SPD  | MII port 5 Speed:Mode<br>10: 1GHz, 01: 100M, 00: 10M<br>(Note: This feature is only valid when port 5 Giga MAC is implemented)                                                                                                                                                                         | 0x0           |
| 4:0   | RO   | SPEED   | Port4 ~ port0 Speed Mode<br>0 : 10M<br>1 : 100M                                                                                                                                                                                                                                                        | 0x0           |

FPA: Force Port4 ~ Port0 Ability (offset: 0x0084)

| Bits  | Type | Name       | Description                                                                                                                                                                          | Initial value |
|-------|------|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:27 | RW   | FORCE_MODE | Port4 ~ port 0 force mode<br>0: default<br>1: force mode. Auto-negotiation status is ignored. All the port ability are forced according to the following fields of the register FPA. | 0x0           |

|       |    |           |                                                                                                                                                                                          |     |
|-------|----|-----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|
| 26:22 | RW | FORCE_LNK | Port 4 ~ port 0 PHY Link<br>This field is valid only FORCE_MDOE is set. The final resolution is reported to POA register.<br>0: link down<br>1: linkup                                   | 0x0 |
| 21    | -  | -         | Reserved                                                                                                                                                                                 | -   |
| 20:16 | RW | FORCE_XFC | Port 4 ~ port 0 Flow control of PHY port<br>This field is valid only FORCE_MDOE is set. The final resolution is reported to POA register.<br>0: default OFF<br>1: 802.3x flow control ON | 0x0 |
| 15:13 | -  | -         | Reserved                                                                                                                                                                                 | -   |
| 12:8  | RW | FORCE_DPX | Port4 ~ port0 Duplex,<br>This field is valid only FORCE_MDOE is set. The final resolution is reported to POA register.<br>0: half duplex<br>1: full duplex                               | 0x0 |
| 7:6   | -  | -         | Reserved                                                                                                                                                                                 | -   |
| 5     | RW | XTAL_COMP | Crystal rate compensation<br>0 : Disable<br>1 : When the switch has transmitted 20000 bytes, the switch will compensate for the loss of crystal rate.                                    | 0x0 |
| 4:0   | RW | FORCE_SPD | Port4 ~ port0 Speed:<br>This field is valid only FORCE_MDOE is set. The final resolution is reported to POA register.<br>0: 10M<br>1: 100M                                               | 0x0 |

PTS: Port Status (offset: 0x0088)

| Bits  | Type | Name          | Description                                                                                                                                                      | Initial value |
|-------|------|---------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:10 | -    | -             | Reserved                                                                                                                                                         | -             |
| 9     | RO   | G1_TXC_STATUS | Port 6 TXC status<br>port 6 TXC status, 1= error, no TXC                                                                                                         | 0x0           |
| 8     | RO   | G0_TXC_STATUS | Port 5 TXC status<br>port 5 TXC status, 1= error, no TXC<br>(Note: This feature is only valid when port 5 Giga MAC is implemented)                               | 0x0           |
| 7     | -    | -             | Reserved                                                                                                                                                         | -             |
| 6:0   | RO   | SECURED_ST    | Security Status<br>1= has intruder coming if turn on the SA_secured mode, read clear<br>(Note: Port5 function is only valid when port 5 Giga MAC is implemented) | 0x0           |

SOCPC: SoC Port Control (offset: 0x008c)

| Bits  | Type | Name        | Description                                                                                                                                                                                                                                    | Initial value |
|-------|------|-------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:26 | -    | -           | Reserved                                                                                                                                                                                                                                       | -             |
| 25    | RW   | CRC_PADDING | CRC padding from CPU<br>If this bit is set , all packets from CPU don't need to append CRC and the outgoing LAN/WAN port will calculate and append CRC.<br>0: packets from CPU need CRC appending<br>1: packets from CPU without CRC appending | 0x1           |

|       |    |                  |                                                                                                                                                                                                                                                                                                                                                                                              |      |
|-------|----|------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|
| 24:23 | RW | CPU_SELECTION-   | CPU Selection<br>00b : Port 6<br>01b : Port 0<br>10b : Port 4<br>11b : Port 5                                                                                                                                                                                                                                                                                                                | 0x0  |
| 22:16 | RW | DISBC2C PU       | When this bit = 1, BC frames from the corresponding port will not be forward to CPU.<br>1'b0 : Includes CPU port.<br>1'b1 : Excludes CPU port<br>(Note: Port5 funciton is only valid when port 5 Giga MAC is implemented)                                                                                                                                                                    | 0x7F |
| 15    | RW | UNI_FCBP_OPTION- | Unicast Frame Flow control/Back pressure option<br>0 : When all ports are fc/bp disable, the switch will use drop_threshold to drop frames only. If not, the switch will use fc_threshold and drop_threshold.<br>1 : When only the destination TX port is fc/bp disable, the switch will use drop_threshold to drop frames only . If not, that TX port uses fc_threshold and drop_threshold. | 0x0  |
| 14:8  | RW | DISMC2C PU       | When this bit =1, MC frames from the corresponding port will not forward to CPU.<br>1'b0 : Includes CPU port.<br>1'b1 : Excludes CPU port<br>(Note: Port5 funciton is only valid when port 5 Giga MAC is implemented)                                                                                                                                                                        | 0x7F |
| 7     | -  | -                | Reserved                                                                                                                                                                                                                                                                                                                                                                                     | -    |
| 6:0   | RW | DISUN2C PU       | When this bit is =1 , unknown UC frames from the corresponding port will not forwarded to CPU<br>1'b0 : Includes CPU port.<br>1'b1 : Excludes CPU port<br>(Note: Port5 funciton is only valid when port 5 Giga MAC is implemented)                                                                                                                                                           | 0x7F |

POC1: Port Control 0 (offset: 0x0090)

| Bits  | Type | Name            | Description                                                                                                                                                                                                          | Initial value |
|-------|------|-----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:30 | RW   | HASH_ADDR_SHIFT | Address table hashing algorithm option for member set index                                                                                                                                                          | 0x0           |
| 29    | RW   | DIS_GMII_PORT_1 | Disable port 6<br>0: port enable<br>1: port disable                                                                                                                                                                  | 0x1           |
| 28    | RW   | DIS_GMII_PORT_0 | Disable port 5<br>0 port enable<br>1: port disable<br>(Note: This feature is only valid when port 5 Giga MAC is implemented)                                                                                         | 0x1           |
| 27:23 | RW   | DIS_PORT        | Disable phy port<br>0: port enable<br>1: port disable                                                                                                                                                                | 0x1F          |
| 22:16 | RW   | DISRMC2 CPU     | Unknown Reserved Multicast Frame Excludes CPU<br>1'b0: Unknown Reserved Multicast Forward Rule (SGC.RMC_RULE)<br>1'b1: Excludes CPU port<br>(Note: Port5 funciton is only valid when port 5 Giga MAC is implemented) | 0x0           |
| 15    | -    | -               | Reserved                                                                                                                                                                                                             | -             |

|      |    |                 |                                                                                                                                                                                                                                                                                                                                                                                            |      |
|------|----|-----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|
| 14:8 | RW | EN_FC           | Apply 802.3x status after Auto-negotiation<br>This field can individually control the 802.3x capability after Auto-negotiation is done.<br>0: ignore the AN stats for 802.3x capability<br>1: follow the AN status for 802.3x capability<br>(Note: Port5 function is only valid when port 5 Giga MAC is implemented)                                                                       | 0x7F |
| 7    | RW | MC_FCBP_OPTION- | Multicast Flow control/Backpressure option<br>0 : When all ports are fc/bp disable, the switch will use drop_threshold to drop frames only. If not, the switch will use fc_threshold and drop_threshold.<br><b>1 : When only the destination TX port is fc/bp disable, switch will use drop_threshold to drop frames only . If not, that TX port uses fc_threshold and drop_threshold.</b> | 0x0  |
| 6:0  | RW | EN_BP           | Apply back pressure capability<br>0: ignore the back pressure mode (default OFF)<br>1: apply back pressure based on SGC.BP_MODE.<br>(Note: Port5 function is only valid when port 5 Giga MAC is implemented)                                                                                                                                                                               | 0x7F |

**POC1: Port Control 1 (offset: 0x0094)**

| Bits  | Type | Name            | Description                                                                                                                                                                                                                                            | Initial value |
|-------|------|-----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:23 | -    | -               | Reserved                                                                                                                                                                                                                                               | -             |
| 29:23 | RW   | DisIPMC2CPU     | Unknown IP Multicast Frame Excludes CPU<br>1'b0: Unknown IP Multicast Forward Rule (SGC.IP_MULT_RULE)<br>1'b1: Excludes CPU port<br>(Note: Port5 function is only valid when port 5 Giga MAC is implemented)                                           | 0x0           |
| 22:16 | RW   | BLOCKING_STATE  | Port State for Spanning Tree Protocol<br>0 : normal state<br>1 : blocking state, forwarding rmc packet to cpu(need programming address table)<br>(Note: Port5 function is only valid when port 5 Giga MAC is implemented)                              | 0x0           |
| 15    | -    | -               | Reserved                                                                                                                                                                                                                                               | -             |
| 14:8  | RW   | DIS_LRNING      | Disable SA learning<br>0: default enabled<br>1: disable Source MAC learning<br>(Note: Port5 function is only valid when port 5 Giga MAC is implemented)                                                                                                | 0x0           |
| 7     | -    | -               | Reserved                                                                                                                                                                                                                                               | 0x0           |
| 6:0   | RW   | SA_SECURED_PORT | SA secured mode<br>0: don't care SA match,<br>1: the packets' SA needs match, otherwise discard the packets<br>(Note: Must set dis_learn and sa_secured at the same time).<br>(Note: Port5 function is only valid when port 5 Giga MAC is implemented) | 0x0           |

**POC2: Port control 2 (offset: 0x0098)**

| Bits | Type | Name         | Description                                                                            | Initial value |
|------|------|--------------|----------------------------------------------------------------------------------------|---------------|
| 31   | -    | -            | Reserved                                                                               | -             |
| 30   | RW   | G1_TXC_CHECK | Check the Port 6 TXC<br>if no txc clock, then disable MII port<br>1: enable, check TXC | 0x0           |

|       |    |                   |                                                                                                                                                                                                                                                                          |      |
|-------|----|-------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|
| 29    | RW | GO_TXC_CHECK      | Check the port 5 TXC<br>if no txc clock, then disable MII port<br>1: enable, check TXC<br>(Note: This feature is only valid when port 5 Giga MAC is implemented)                                                                                                         | 0x0  |
| 28:26 | -  | -                 | Reserved                                                                                                                                                                                                                                                                 | -    |
| 25    | RW | MLD2CPU_EN        | MLD Message Packets forward to CPU<br>1'b0 : MLD message will be flooded to all ports                                                                                                                                                                                    | 0x0  |
| 24:23 | RW | IPV6_MULT_RULE    | Unknown IPV6 Multicast Frame Forward Rule<br>If no match in the address table, then following the rule<br>00: BC<br>01: to cpu<br>10: drop<br>11: Reserved                                                                                                               | 0x0  |
| 22:16 | RW | DIS_UC_PAUSE      | Disable Unicast Pause Frame<br>0: switch will consider pause frame when DA!=0180c20001 but unicast to CPU,<br>1: switch will not consider pause frame when DA!=0180c20001 and unicast to CPU<br>(Note: Port5 function is only valid when port 5 Giga MAC is implemented) | 0x0  |
| 15    | RW | PER_VLAN_UNTAG_EN | Per port per vlan untag enable<br>VLAN tag removal option.<br>0 : Use per port UNTAG_EN<br>1 : Use untag enable bitmap in VLAN table                                                                                                                                     | 0x0  |
| 14:8  | RW | ENAGING PORT      | Port aging<br>0: disable aging that the MAC address is belong to programmed port(s)<br>1: enable aging<br>(Note: Port5 function is only valid when port 5 Giga MAC is implemented)                                                                                       | 0x7F |
| 7     | -  | -                 | Reserved                                                                                                                                                                                                                                                                 | -    |
| 6:0   | RW | UNTAG_EN          | Per Port VLAN Tag Removal<br>0: disable<br>1: enable VLAN tag field removal.<br>(Note: Port5 function is only valid when port 5 Giga MAC is implemented)                                                                                                                 | 0x0  |

SGC: Switch Global Control (offset: 0x009c)

| Bits | Type | Name        | Description                                                                                                                                                                                | Initial value |
|------|------|-------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31   | -    | -           | Reserved                                                                                                                                                                                   | -             |
| 30   | RW   | BKOFF_ALG   | Backoff Algorithm Option<br>0: default<br>1: comply with UNH test                                                                                                                          | 0x1           |
| 29   | RW   | LEN_ERR_CHK | Length of Received Frame Check Enable<br>When the bit is set, the received packet length will be checked for length encapsulated frames.<br>0: default disabled<br>1: comply with UNH test | 0x1           |

|       |    |                    |                                                                                                                                                                                                                         |     |
|-------|----|--------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|
| 28:27 | RW | IP_MULT_RULE       | Unknown IP Multicast Frame Forward Rule<br>If no match in the address table, then following the rules,<br>00: BC<br>01: to cpu<br>10: drop<br>11: reserved                                                              | 0x0 |
| 26:25 | RW | RMC_RULE           | Unknown Reserved Multicast Frame Forward Rule<br>If no match in the address table, then follow the rules,<br>00: to all port(not include blocking state port)<br>01: to cpu<br>10: drop<br>11: reserved                 | 0x0 |
| 24:23 | RW | LED_FLASH_TIME     | The Frequency Of LED Flash<br>00: 30ms<br>01: 60ms<br>10: 240ms<br>11: 480ms                                                                                                                                            | 0x0 |
| 22:21 | RW | BISH_TH            | The Threshold Of Memory Bisshop<br>11:skip if fail 8 blocks, 0<br>00:skip if fail 16 (default, from pins)<br>01:skip if fail 48<br>10:skip if fail 64                                                                   | 0x0 |
| 20    | RO | BISH_DIS           | Build In Self Hop<br>0: enable skip function (default, from pin)                                                                                                                                                        | 0x0 |
| 19:18 | RW | BP_MODE            | Back Pressure Mode<br>00: disable<br>01: BP jam, the jam number is set by bp_num<br>10: BP jamALL, jam packet until the BP condition is released(default),<br>11: BP carrier, use carrier insertion to do back pressure | 0x2 |
| 17:16 | RW | DISMIIPORT_WASTX   | GMII Port Disable Was_Transmit<br>1: disable was_transmit (good for late CRS PHY, like HPNA2.0 or power-LAN),<br>0: enable<br>(Note: This feature is only valid when port 5 Giga MAC is implemented)                    | 0x0 |
| 15:12 | RW | BP_JAM_CNT         | Back Pressure Jam Number<br>The consecutive jam count when back pressure is enabled, The default is 10 packet jam then one no-jam packet.                                                                               | 0xA |
| 11    | RW | DISABLE_TX_BACKOFF | Disable The Collision Back Off Timer<br>0: default<br>1: re-transmit immediately after collision,                                                                                                                       | 0x0 |
| 10:9  | RW | ADDRESS_HASH_ALG   | MAC Address Hashing Algorithm<br>00: direct mode, using last 10-bit as hashing address<br>01: XOR48 mode<br>10: XOR32 mode<br>11:reserved                                                                               | 0x0 |
| 8     | RW | DIS_PKT_TX_ABORT   | Disable Packet TX Abort<br>1: Disable collision 16 packet abort and late collision abort<br>0: enable both abort                                                                                                        | 0x0 |



|     |    |                |                                                                                                                                                                     |            |            |     |
|-----|----|----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|------------|-----|
| 7:6 | RW | PKT_MAX_LEN    | Maximum Packet Length                                                                                                                                               |            |            | 0x1 |
|     |    |                |                                                                                                                                                                     | Untaged    | VLAN-taged |     |
|     |    |                | 00b                                                                                                                                                                 | 1536 Bytes | 1536 Bytes |     |
|     |    |                | 01b                                                                                                                                                                 | 1518 Bytes | 1522 Bytes |     |
|     |    |                | 10b                                                                                                                                                                 | 1522 Bytes | 1526 Bytes |     |
|     |    |                | 11b                                                                                                                                                                 | Reserved   | Reserved   |     |
| 5:4 | RW | BC_STORM_PROT  | Global Broadcast Storm Protection<br>BC will be blocked, if the following number of BC blocks in output queues<br><u>00: disable</u><br>01: 64<br>10: 96<br>11: 128 |            |            | 0x0 |
| 3:0 | RW | AGING INTERVAL | Aging Timer<br>0000: disable age<br>0001: 300sec<br>0010 ~ 0111: 600 ~ 38400sec<br>1xxx: Fast Age (60sec)                                                           |            |            | 0x1 |

STRT: Switch Reset (offset: 0x00a0)

| Bits | Type | Name     | Description                                                                                                          | Initial value |
|------|------|----------|----------------------------------------------------------------------------------------------------------------------|---------------|
| 31:0 | WO   | Reset_SW | Reset switch engine, data, address, link memory , cpu port and ahb interface when writing data to the STRT register. | 0x0           |

LEDPO: LED Port0 (offset: 0x00a4)

| Bits | Type | Name   | Description                                                                                                                                                                                                                                                                                                           | Initial value |
|------|------|--------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:4 | -    | -      | Reserved                                                                                                                                                                                                                                                                                                              | -             |
| 3:0  | RW   | P0_LED | port0 LED state, default = link/activity<br>4'b0000: link<br>4'b0001: 100M speed<br>4'b0010: duplex<br>4'b0011: activity<br>4'b0100: collision<br>4'b0101: link/activity<br>4'b0110: duplex/collision<br>4'b0111: 10M speed/activity<br>4'b1000: 100M speed/activity<br>4'b1011: off<br>4'b1100: on<br>4'b1010: blink | 0x5           |

LEDPI: LED Port 1 (offset: 0x00a8)

| Bits | Type | Name   | Description                              | Initial value |
|------|------|--------|------------------------------------------|---------------|
| 31:4 | -    | -      | Reserved                                 | -             |
| 3:0  | RW   | P1_LED | Port1 LED state, default = link/activity | 0x5           |

LEDPI: LED Port2 (offset: 0x00ac)

| Bits | Type | Name   | Description                              | Initial value |
|------|------|--------|------------------------------------------|---------------|
| 31:4 | -    | -      | Reserved                                 | -             |
| 3:0  | RW   | P2_LED | Port2 LED state, default = link/activity | 0x5           |

LEDPI: LED Port3 (offset: 0x00b0)

| Bits | Type | Name   | Description                              | Initial value |
|------|------|--------|------------------------------------------|---------------|
| 31:4 | -    | -      | Reserved                                 | -             |
| 3:0  | RW   | P3_LED | Port3 LED state, default = link/activity | 0x5           |

LEDPI: LED Port4 (offset: 0x00b4)



| Bits | Type | Name   | Description                              | Initial value |
|------|------|--------|------------------------------------------|---------------|
| 31:4 | -    | -      | Reserved                                 | -             |
| 3:0  | RW   | P4_LED | Port4 LED state, default = link/activity | 0x5           |

WDTR: Watch Dog trigger Reset (offset: 0x00b8)

| Bits | Type | Name         | Description                                                                                                                                  | Initial value |
|------|------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:8 | -    | -            | Reserved                                                                                                                                     | -             |
| 7:0  | RW   | BUF_STARV_TH | <b>Buffer starvation threshold</b><br>Switch will interrupt CPU when the global queue block counts is less than the threshold for 3 seconds. | 0x1E          |

DES: Debug Signal (offset: 0x00bc)

| Bits  | Type | Name         | Description         | Initial value |
|-------|------|--------------|---------------------|---------------|
| 31:16 | -    | -            | Reserved            | 0x0           |
| 15:0  | RO   | DEBUG_SIGNAL | Port 5 debug signal | 0x0           |

PCR0: PHY Control Register 0 (offset: 0x00c0)

| Bits  | Type | Name             | Description                                                                                                                                                                                                                                       | Initial value |
|-------|------|------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:16 | RW   | WT_NWAY_DATA     | The data be written into the PHY                                                                                                                                                                                                                  | 0x0           |
| 15    | -    | -                | Reserved                                                                                                                                                                                                                                          | -             |
| 14    | RW   | RD_PHY_CMD       | Read command<br>To enable read command on PHY, write 1 to this bit . After command is completed, this bit is self-cleared.                                                                                                                        | 0x0           |
| 13    | RW   | WT_PHY_CMD       | Write command<br>To enable write command on PHY, write 1 to this bit . After command is completed, this bit is self-cleared                                                                                                                       | 0x0           |
| 12:8  | RW   | CPU_PHY_REG_ADDR | PHY register address                                                                                                                                                                                                                              | 0x0           |
| 7:5   | -    | -                | Reserved                                                                                                                                                                                                                                          | 0x0           |
| 4:0   | RW   | CPU_PHY_ADDR     | PHY address<br>(Note: The internal 5-ports PHY reserves the PHY address starting from 5'd0 ~ 5'd4. For the external PHY, the PHY address from 5'd5 to 5'd31 can be applied. The default PHY address of Port 5 is 5'd5 for auto-polling function.) | 0x0           |

PCR1: PHY control register 1 (offset: 0x00c4)

| Bits  | Type | Name    | Description                         | Initial value |
|-------|------|---------|-------------------------------------|---------------|
| 31:16 | RO   | RD_DATA | The Read Data                       | 0x0           |
| 15:2  | -    | -       | Reserved                            | -             |
| 1     | RO   | RD_RDY  | Read operation is done, read clear  | 0x0           |
| 0     | RO   | WT_DONE | Write operation is done, read clear | 0x0           |

FPA1: Force Port 5 ~Port 6 ability (offset: 0x00c8)

| Bits  | Type | Name              | Description                                                                                                | Initial value |
|-------|------|-------------------|------------------------------------------------------------------------------------------------------------|---------------|
| 31:30 | -    | -                 | Reserved                                                                                                   | -             |
| 29    | RW   | AP_EN             | Port 5 Auto polling enable<br>(Note: This feature is only valid when port 5 Giga MAC is implemented)       | 0x0           |
| 28:24 | RW   | EXT_PHY_ADDR_BASE | Port 5 External phy base address<br>(Note: This feature is only valid when port 5 Giga MAC is implemented) | 0x5           |
| 23:22 | RW   | GO_RXCLK_SKEW_SEL | Port 5 rxclock skew selection<br>(Note: This feature is only valid when port 5 Giga MAC is implemented)    | 0x1           |
| 21:20 | RW   | GO_TXCLK_MODE_SEL | Port 5 txclock skew selection<br>(Note: This feature is only valid when port 5 Giga MAC is implemented)    | 0x1           |

|       |    |                   |                                                                                                                                                                                                                                                    |     |
|-------|----|-------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|
| 19    | -  | -                 | Reserved                                                                                                                                                                                                                                           | 0x0 |
| 18    | RW | TURBO_MII_CLK     | Port 5 revMII mode clock selection<br>0 : 25MHz output clock<br>1 : 31.25MHz output clock<br>(Note: This feature is only valid when port 5 Giga MAC is implemented)                                                                                | 0x0 |
| 17:14 | -  | -                 | Reserved                                                                                                                                                                                                                                           | -   |
| 13    | RW | FORCE_RGMII_LINK1 | Force port 6 link<br>This field is valid only FORCE_MDOE is set. The final resolution is reported to POA register.<br>0: link down<br>1: link up                                                                                                   | 0x0 |
| 12    | RW | FORCE_RGMII_LINK0 | Force port 5 link<br>This field is valid only FORCE_MDOE is set. The final resolution is reported to POA register.<br>0: link down<br>1: link up<br>(Note: This feature is only valid when port 5 Giga MAC is implemented)                         | 0x0 |
| 11    | RW | FORCE_RGMII_EN1   | Force port 6 enable<br>0: reserved<br>1: force mode. Auto-negotiation status is ignored. Port 6 ability is forced according to the following fields of register FPA1.                                                                              | 0x0 |
| 10    | RW | FORCE_RGMII_EN0   | Force port 5 enable<br>0: default<br>1: force mode. Auto-negotiation status is ignored. Port 5 ability is forced according to the following fields of the register FPA1.<br>(Note: This feature is only valid when port 5 Giga MAC is implemented) | 0x0 |
| 9:8   | RW | FORCE_RGMII_XFC1  | Force port 6 flow control ability<br>This field is valid only FORCE_MDOE is set. The final resolution is reported to POA register.<br>1x: for tx<br>x1: for rx                                                                                     | 0x3 |
| 7:6   | RW | FORCE_RGMII_XFC0  | Force port 5 flow control ability<br>This field is valid only FORCE_MDOE is set. The final resolution is reported to POA register.<br>1x: for tx<br>x1: for rx<br>(Note: This feature is only valid when port 5 Giga MAC is implemented)           | 0x0 |
| 5     | RW | FORCE_RGMII_DPX1  | Force port 6 duplex<br>This field is valid only FORCE_MDOE is set. The final resolution is reported to POA register.<br>0: half duplex<br>1: full duplex                                                                                           | 0x1 |
| 4     | RW | FORCE_RGMII_DPX0  | Force port 5 duplex<br>This field is valid only FORCE_MDOE is set. The final resolution is reported to POA register.<br>0: half duplex<br>1: full duplex<br>(Note: This feature is only valid when port 5 Giga MAC is implemented)                 | 0x0 |

|     |    |                  |                                                                                                                                                                                                                                      |     |
|-----|----|------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|
|     |    |                  | implemented)                                                                                                                                                                                                                         |     |
| 3:2 | RW | FORCE_RGMII_SPD1 | Force port 6 speed<br>This field is valid only FORCE_MDOE is set. The final resolution is reported to POA register.<br>1x: 1Gbps<br>01: 100Mbps<br>00: 10Mbps                                                                        | 0x2 |
| 1:0 | RW | FORCE_RGMII_SPD0 | Force port 5 speed<br>This field is valid only FORCE_MDOE is set. The final resolution is reported to POA register.<br>1x: 1Gbps<br>01: 100Mbps<br>00: 10Mbps<br>(Note: This feature is only valid when port 5 Giga MAC implemented) | 0x0 |

**FCT2: Flow Control Threshold 2 (offset: 0x00cc)**

| Bits  | Type | Name             | Description                                                                                                                                                                                                                      | Initial value |
|-------|------|------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:25 | -    | -                | Reserved                                                                                                                                                                                                                         | -             |
| 24:18 | RW   | DIS_IPV6MC2CPU   | Unknown IPv6 Multicast Frame Excludes CPU<br>1'b0: Unknown IPv6 Multicast Forward Rule (POC2.IPV6_MULT_RULE)<br>1'b1: Excludes CPU port                                                                                          | 0x0           |
| 17:13 | RW   | MUST_DROP_RLS_TH | If the global queue pointer higher than the threshold. The must drop condition will be released.                                                                                                                                 | 0x5           |
| 12:8  | RW   | MUST_DROP_SET_TH | If the global queue pointer reach must drop. All incoming packets have to be dropped.                                                                                                                                            | 0x3           |
| 7:6   | -    | -                | Reserved                                                                                                                                                                                                                         | -             |
| 5:0   | RW   | MC_PER_PORT_TH   | MC packets per port threshold.<br>When the global queue reaches the flow control threshold on register FCT0, per port output threshold for MC packet will be checked to enable flow-control or packet-dop on incoming MC packet. | 0xC           |

**QSS0: Queue\_Status\_0 (offset: 0x00d0)**

| Bits  | Type | Name             | Description                                          | Initial value |
|-------|------|------------------|------------------------------------------------------|---------------|
| 31:24 | -    | -                | Reserved                                             | -             |
| 23:15 | RO   | BE_CNT_R         | Link control best effort queue block counter monitor | 0x0           |
| 14:5  | RO   | BK_CNT_R         | Link control background queue block counter monitor  | 0x0           |
| 4:0   | RW   | SEE_CNT_PORT_SEL | Link control block counter port selection            | 0x0           |

**QSS1: Queue\_Status\_1 (offset: 0x00d4)**

| Bits  | Type | Name     | Description                                           | Initial value |
|-------|------|----------|-------------------------------------------------------|---------------|
| 31:18 | -    | -        | Reserved                                              | -             |
| 17:9  | RO   | VO_CNT_R | Link control voice queue block counter monitor        | 0x0           |
| 8:0   | RO   | CL_CNT_R | Link control control load queue block counter monitor | 0x0           |

**DEC: Debug Control (offset: 0x00d8)**

| Bits  | Type | Name             | Description                                                                                                              | Initial value |
|-------|------|------------------|--------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:24 | RW   | SW2FE_BRIDGE_IPG | SW2FE Bridge IPG Byte Count<br>Inter-Frame Byte Count between the consecutive frames flowing from Switch to Frame Engine | 0x40          |
| 23:16 | RW   | FE2SW_BRIDGE_IPG | FE2SW Bridge IPG byte count<br>Inter-Frame Byte Count between the consecutive frames flowing from Frame Engine to Switch | 0x40          |

|      |    |                   |                                                                                                                                                          |     |
|------|----|-------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------|-----|
| 15:9 | -  | -                 | Reserved                                                                                                                                                 | -   |
| 8    | RW | BRIDGE_EN         | Enable FE2SW Bridge IPG Prevention<br>1'b0: Disable<br>1'b1: Enable IPG Prevention when FE2SW_BRIDGE_IPG is too short (8'd16) to receive the next frame. | 0x1 |
| 7:6  | -  | -                 | Reserved                                                                                                                                                 | -   |
| 5:3  | RW | DEBUG_SW_PORT_SEL | Port 5 debug selection control<br>(Note: This feature is only valid when port 5 Giga MAC is implemented)                                                 | 0x0 |
| 2:0  | -  | -                 | Reserved                                                                                                                                                 | -   |

**MTI: Memory Test Information (offset: 0x00dc)**

| Bits  | Type | Name             | Description                                                                                     | Initial value |
|-------|------|------------------|-------------------------------------------------------------------------------------------------|---------------|
| 31:16 | -    | -                | Reserved                                                                                        | -             |
| 15:7  | RO   | SKIP_BLOCKS      | Skip block counter<br>This field indicates how many blocks are skipped due to memory bit fault. | 0x0           |
| 6     | RS   | SW_MEM_TEST_DONE | Switch memory test done                                                                         | 0x0           |
| 5     | RS   | LK_RAM_TEST_DONE | Link ram test done                                                                              | 0x0           |
| 4     | RO   | LK_RAM_TEST_FAIL | Link ram test fail                                                                              | 0x0           |
| 3     | RS   | AT_RAM_TEST_DONE | Address table ram test done                                                                     | 0x0           |
| 2     | RO   | AT_RAM_TEST_FAIL | Address table ram test fail                                                                     | 0x0           |
| 1     | RS   | DT_RAM_TEST_DONE | Data buffer ram test done                                                                       | 0x0           |
| 0     | RO   | DT_RAM_TEST_FAIL | Data buffer ram test fail                                                                       | 0x0           |

**PPC: Port 6 Packet Counter (offset: 0x00e0)**

| Bits  | Type | Name      | Description                           | Initial value |
|-------|------|-----------|---------------------------------------|---------------|
| 31:16 | RO   | SW2FE_CNT | Switch to frame engine packet counter | 0x0           |
| 15:0  | RO   | FE2SW_CNT | Frame engine to switch packet counter | 0x0           |

**SGC2: Switch Global Control 2 (offset: 0x00e4)**

| Bits  | Type | Name           | Description                                                                                                                                                                                                                            | Initial value |
|-------|------|----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31    | RW   | P6_RXFC_QUE_EN | Port 6 RX flow control on per egress queue<br>0: Port 6 RX flow control will pause all 4 egress queue<br>1: Port 6 RX flow control will pause 4 egress queue independently according to the corresponding congestion signals.          | 0x0           |
| 30    | RW   | P6_TXFC_WL_EN  | Port 6 TX flow controll by Switch WAN/LAN port<br>0: Port 6 TX flow control is decided by any port and any queue of the Switch congestion<br>1: Port 6 TX flow control is decided by WAN/LAN port of the Switch congestion separately. | 0x0           |
| 29:24 | RW   | LAN_PMAP       | Lan port bit map<br>This field indicates per port attribute used for flow control.<br>1: Lan port<br>0: Wan port<br>(Note: Port5 funciton is only valid when port 5 Giga MAC is implemented)                                           | 0x0           |

|       |    |                     |                                                                                                                                                                                                                                                                                                                                                           |     |
|-------|----|---------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|
| 23    | RW | SPECIAL_TAG_EN      | Special Tag enable<br>0 : default<br>RX special tag is enabled according to the global control bit- CPU_TPID_EN<br>TX special tag is enabled according to the per-port TX_CPU_TPID_BIT_MAP<br>1 : CPU_TPID_EN is not used<br>Both TX and RX special tag feature are decided by the per-port TX_CPU_TPID_BIT_MAP                                           | 0x0 |
| 22:16 | RW | TX_CPU_TPID_BIT_MAP | Transmit CPU TPID(810x) port bit map<br>0: default (TPID=0x8100)<br>1: TPID=0x810? depending on TX/RX usages<br>(Note: Port5 function is only valid when port 5 Giga MAC is implemented)                                                                                                                                                                  | 0x0 |
| 15:13 | -  | -                   | Reserved                                                                                                                                                                                                                                                                                                                                                  | -   |
| 12    | RW | P6_TXFC_QUE_EN      | Port 6 per queue TX flow control<br>This bit is only valid when P6_TXFC_WL_EN is enabled.<br>0 : 4 congest signals to Frame Engine are decided by the wired-or result of all egress queues on Switch WAN/LAN ports.<br>1 : 4 congest signals to Frame Engine are decided by the individual and the corresponding 4 egress queues on Switch WAN/LAN ports. | 0x0 |
| 11    | RW | ARBITER_LAN_EN      | Memory arbiter only for P0~P4 enable<br>0: default<br>1: memory arbiter only for P0~P4.                                                                                                                                                                                                                                                                   | 0x0 |
| 10    | RW | CPU_TPID_EN         | CPU TPID(81xx) enable<br>0: disable. CPU TPID=8100<br>1: enable. CPU TPID=810x.                                                                                                                                                                                                                                                                           | 0x0 |
| 9     | RW | ARBITER_GPT_EN      | Memory Arbiter only for P5 and P6<br>0: default<br>1: enable                                                                                                                                                                                                                                                                                              | 0x0 |
| 8     | RW | SLOT_4TO1           | Memory Arbiter Ratio Selection<br>0: (P5,P6) : (P0-P4) = 3:2<br>1: (P5,P6) : (P0-P4) = 4:1                                                                                                                                                                                                                                                                | 0x0 |
| 7     | -  | -                   | Reserved                                                                                                                                                                                                                                                                                                                                                  | -   |
| 6:0   | RW | DOUBLE_TAG_EN       | Insert double tag field<br>When this bit is set , the incoming packet is allowed to insert outer or double tag.<br>1: enable double tag field<br>0: disable the double tag field.<br>(Note: Port5 function is only valid when port 5 Giga MAC is implemented)                                                                                             | 0x0 |

**POP0: Port 0 Packet Counter (offset: 0x00e8)**

| Bits  | Type | Name          | Description                        | Initial value |
|-------|------|---------------|------------------------------------|---------------|
| 31:16 | RO   | BAD_PKT_CNT0  | Port 0 receive bad packet counter  | 0x0           |
| 15:0  | RO   | GOOD_PKT_CNT0 | Port 0 receive good packet counter | 0x0           |

**P1PC: Port 1 Packet Counter (offset: 0x00ec)**

| Bits  | Type | Name          | Description                        | Initial value |
|-------|------|---------------|------------------------------------|---------------|
| 31:16 | RO   | BAD_PKT_CNT1  | Port 1 receive bad packet counter  | 0x0           |
| 15:0  | RO   | GOOD_PKT_CNT1 | Port 1 receive good packet counter | 0x0           |

**P2PC: Port 2 Packet Counter (offset: 0x00f0)**

| Bits | Type | Name | Description | Initial value |
|------|------|------|-------------|---------------|
|------|------|------|-------------|---------------|

|       |    |               |                                    |     |
|-------|----|---------------|------------------------------------|-----|
| 31:16 | RO | BAD_PKT_CNT2  | Port 2 receive bad packet counter  | 0x0 |
| 15:0  | RO | GOOD_PKT_CNT2 | Port 2 receive good packet counter | 0x0 |

P3PC: Port 3 Packet Counter (offset: 0x00f4)

| Bits  | Type | Name          | Description                        | Initial value |
|-------|------|---------------|------------------------------------|---------------|
| 31:16 | RO   | BAD_PKT_CNT3  | Port 3 receive bad packet counter  | 0x0           |
| 15:0  | RO   | GOOD_PKT_CNT3 | Port 3 receive good packet counter | 0x0           |

P4PC: Port 4 packet counter (offset: 0x00f8)

| Bits  | Type | Name          | Description                        | Initial value |
|-------|------|---------------|------------------------------------|---------------|
| 31:16 | RO   | BAD_PKT_CNT4  | Port 4 receive bad packet counter  | 0x0           |
| 15:0  | RO   | GOOD_PKT_CNT4 | Port 4 receive good packet counter | 0x0           |

P5PC: Port 5 packet counter (offset: 0x00fc)

| Bits  | Type | Name          | Description                                                                                                  | Initial value |
|-------|------|---------------|--------------------------------------------------------------------------------------------------------------|---------------|
| 31:16 | RO   | BAD_PKT_CNT5  | Port 5 receive bad packet counter<br>(Note: This feature is only valid when port 5 Giga MAC is implemented)  | 0x0           |
| 15:0  | RO   | GOOD_PKT_CNT5 | Port 5 receive good packet counter<br>(Note: This feature is only valid when port 5 Giga MAC is implemented) | 0x0           |

VUB0: VLAN Untag Block 0 (offset: 0x0100)

| Bits  | Type | Name            | Description                                                                                               | Initial value |
|-------|------|-----------------|-----------------------------------------------------------------------------------------------------------|---------------|
| 31:28 | -    | -               | Reserved                                                                                                  | -             |
| 27:21 | RW   | VLAN_3_UNTAG_EN | Port 0 ~ 6 untag_en of VLAN 3<br>(Note: Port5 function is only valid when port 5 Giga MAC is implemented) | 0x0           |
| 20:14 | RW   | VLAN_2_UNTAG_EN | Port 0 ~ 6 untag_en of VLAN 2                                                                             | 0x0           |
| 13:7  | RW   | VLAN_1_UNTAG_EN | Port 0 ~ 6 untag_en of VLAN 1                                                                             | 0x0           |
| 6:0   | RW   | VLAN_0_UNTAG_EN | Port 0 ~ 6 untag_en of VLAN 0                                                                             | 0x0           |

VUB0: VLAN Untag Block 1 (offset: 0x0104)

| Bits  | Type | Name            | Description                   | Initial value |
|-------|------|-----------------|-------------------------------|---------------|
| 31:28 | -    | -               | Reserved                      | -             |
| 27:21 | RW   | VLAN_7_UNTAG_EN | Port 0 ~ 6 untag_en of VLAN 7 | 0x0           |
| 20:14 | RW   | VLAN_6_UNTAG_EN | Port 0 ~ 6 untag_en of VLAN 6 | 0x0           |
| 13:7  | RW   | VLAN_5_UNTAG_EN | Port 0 ~ 6 untag_en of VLAN 5 | 0x0           |
| 6:0   | RW   | VLAN_4_UNTAG_EN | Port 0 ~ 6 untag_en of VLAN 4 | 0x0           |

VUB0: VLAN Untag Block 2 (offset: 0x0108)

| Bits  | Type | Name             | Description                    | Initial value |
|-------|------|------------------|--------------------------------|---------------|
| 31:28 | -    | -                | Reserved                       | -             |
| 27:21 | RW   | VLAN_11_UNTAG_EN | Port 0 ~ 6 untag_en of VLAN 11 | 0x0           |
| 20:14 | RW   | VLAN_10_UNTAG_EN | Port 0 ~ 6 untag_en of VLAN 10 | 0x0           |

|      |    |                 |                               |     |
|------|----|-----------------|-------------------------------|-----|
| 13:7 | RW | VLAN_9_UNTAG_EN | Port 0 ~ 6 untag_en of VLAN 9 | 0x0 |
| 6:0  | RW | VLAN_8_UNTAG_EN | Port 0 ~ 6 untag_en of VLAN 8 | 0x0 |

**VUB0: VLAN Untag Block 3 (offset: 0x010c)**

| Bits  | Type | Name             | Description                    | Initial value |
|-------|------|------------------|--------------------------------|---------------|
| 31:28 | -    | -                | Reserved                       | -             |
| 27:21 | RW   | VLAN_15_UNTAG_EN | Port 0 ~ 6 untag_en of VLAN 15 | 0x0           |
| 20:14 | RW   | VLAN_14_UNTAG_EN | Port 0 ~ 6 untag_en of VLAN 14 | 0x0           |
| 13:7  | RW   | VLAN_13_UNTAG_EN | Port 0 ~ 6 untag_en of VLAN 13 | 0x0           |
| 6:0   | RW   | VLAN_12_UNTAG_EN | Port 0 ~ 6 untag_en of VLAN 12 | 0x0           |

**BMU\_CTRL: Broadcast/Multicast/Unknown Rate Limit Control (offset: 0x0110)**

| Bits  | Type | Name               | Description                                                                                                             | Initial value |
|-------|------|--------------------|-------------------------------------------------------------------------------------------------------------------------|---------------|
| 31    | -    | -                  | Reserved                                                                                                                | -             |
| 30:24 | RW   | ONE_US_CYCLE_NUM   | One micro-second cycle number<br>This field is used to calculate 1us period.                                            | 0x7C          |
| 23    | -    | -                  | Reserved                                                                                                                | -             |
| 22:20 | RW   | P5_RATE_LIMIT_CTRL | Port 5 rate limit control<br>(Note: This feature is only valid when port 5 Giga MAC is implemented)                     | 0x0           |
| 19    | -    | -                  | Reserved                                                                                                                | -             |
| 18:16 | RW   | P4_RATE_LIMIT_CTRL | Port 4 rate limit control                                                                                               | 0x0           |
| 15    | -    | -                  | Reserved                                                                                                                | -             |
| 14:12 | RW   | P3_RATE_LIMIT_CTRL | Port 3 rate limit control                                                                                               | 0x0           |
| 11    | -    | -                  | Reserved                                                                                                                | -             |
| 10:8  | RW   | P2_RATE_LIMIT_CTRL | Port 2 rate limit control                                                                                               | 0x0           |
| 7     | -    | -                  | Reserved                                                                                                                | -             |
| 6:4   | RW   | P1_RATE_LIMIT_CTRL | Port 1 rate limit control                                                                                               | 0x0           |
| 3     | -    | -                  | Reserved                                                                                                                | -             |
| 2:0   | RW   | P0_RATE_LIMIT_CTRL | Port 0 rate limit control<br>[2] : Broadcast frame enable<br>[1] : Multicast frame enable<br>[0] : Unknown frame enable | 0x0           |

**BMU\_LMT\_NUM\_1: Broadcast/Multicast/Unknown Rate Limit Frame Number 1 (offset: 0x0114)**

| Bits  | Type | Name                   | Description                                                                                 | Initial value |
|-------|------|------------------------|---------------------------------------------------------------------------------------------|---------------|
| 31:16 | RW   | RATE_LIMIT_NUMBER_100M | Rate Limit received Broadcast / Multicast / Unknown frame number in 100M in 100 ms duration | 0xFFFF        |
| 15:0  | RW   | RATE_LIMIT_NUMBER_10M  | Rate Limit received Broadcast / Multicast / Unknown frame number in 10M in 1 sec duration.  | 0xFFFF        |



**RL\_NUM\_10M: Rate Limit Frame Number 2 (offset: 0x0118)**

| Bits  | Type | Name                     | Description                                                                                                                                                           | Initial value |
|-------|------|--------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31    | RW   | INGRESS_RATE_BYTE_OPTION | Ingress Rate Byte Option<br>0 : Add<br>1 : Minus                                                                                                                      | 0x0           |
| 30:24 | RW   | INGRESS_RATE_BYTE_NUM    | Ingress Rate Byte number                                                                                                                                              | 0x18          |
| 23    | RW   | EGRESS_RATE_BYTE_OPTION  | Egress Rate Byte Option<br>0 : Add<br>1 : Minus                                                                                                                       | 0x0           |
| 22:16 | RW   | EGRESS_RATE_BYTE_NUM     | Egress Rate Byte number                                                                                                                                               | 0x18          |
| 15:0  | RW   | RATE_LIMIT_NUMBER_1000M  | Rate Limit received Broadcast / Multicast / Unknown frame number in 1000M in 10 ms duration<br>(Note: This feature is only valid when port 5 Giga MAC is implemented) | 0xFFFF        |

**P01\_ING\_CTRL: Port 0 & 1 Ingress Rate Limit Control(offset: 0x011c)**

| Bits  | Type | Name                    | Description                                                                                                                                                                                                                                                                               | Initial value |
|-------|------|-------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31    | -    | -                       | Reserved                                                                                                                                                                                                                                                                                  | -             |
| 30    | RW   | P1_INGRESS_CTRL         | P1 Ingress Limit Control<br>1:ON<br>0:OFF                                                                                                                                                                                                                                                 | 0x0           |
| 29    | RW   | P1_MNG_PKT_BYPASS       | P1 Management Packet Bypass<br>Per packet dropped by ingress rate limit, the management frames can be ignored when the bit is set.<br>(Only bypass BPDUs, IGMP & MLD packets)<br>0: all packet included<br>1: Management Frame excluded                                                   | 0x0           |
| 28    | RW   | P1_INGRESS_FLOW_CTRL_ON | Port 1 Ingress rate flow control<br>When the bit is set, the pause frame is used prior to packet dropped according to P1_ING_THRES. If the bucket is empty, then P1 will start to discard the received packets except those specific packet in P1_MNG_PKT_BYPASS mode.<br>0: OFF<br>1: ON | 0x0           |
| 27:26 | RW   | P1_TIMER_TICK           | Port 1 Timer Tick<br>0 : 512 us<br>1 : 128 us<br>2 : 32 us<br>3 : 8 us                                                                                                                                                                                                                    | 0x0           |
| 25:16 | RW   | P1_TOKEN                | Port 1 Token<br>Every timer tick, Token number bytes will be added into the bucket. (Unit : Byte)<br>The maximum space of this bucket is 16'hFFFF bytes                                                                                                                                   | 0x0           |
| 15    | -    | -                       | Reserved                                                                                                                                                                                                                                                                                  | -             |
| 14    | RW   | P0_INGRESS_CTRL         | P0 Ingress Limit Control<br>1:ON<br>0:OFF                                                                                                                                                                                                                                                 | 0x0           |



|       |    |                             |                                                                                                                                                                                                                                                                                           |     |
|-------|----|-----------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|
| 13    | RW | P0_MNG_PKT_BY<br>PASS       | P0 Management Packet Bypass<br>Per packet dropped by ingress rate limit, the management frames can be ignored when the bit is set.<br>(Only bypass BPDUs, IGMP & MLD packets)<br>0: all packet included<br>1: Management Frame excluded                                                   | 0x0 |
| 12    | RW | P0_INGRESS_FLO<br>W_CTRL_ON | Port 0 Ingress rate flow control<br>When the bit is set, the pause frame is used prior to packet dropped according to P0_ING_THRES. If the bucket is empty, then P0 will start to discard the received packets except those specific packet in P0_MNG_PKT_BYPASS mode.<br>0: OFF<br>1: ON | 0x0 |
| 11:10 | RW | P0_TIMER_TICK               | Port 0 Timer Tick<br>0 : 512 us<br>1 : 128 us<br>2 : 32 us<br>3 : 8 us                                                                                                                                                                                                                    | 0x0 |
| 9:0   | RW | P0_TOKEN                    | Port 0 Token<br>Every timer tick, Token number bytes will be added into the bucket. (Unit : Byte)<br>The maximum space of the bucket is 16'hFFFF bytes.                                                                                                                                   | 0x0 |

**P23\_ING\_CTRL: Port 2 & 3 Ingress Rate Limit Control(offset: 0x0120)**

| Bits  | Type | Name                        | Description                                                                                                                                                                                                                                                                               | Initial value |
|-------|------|-----------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31    | -    | -                           | Reserved                                                                                                                                                                                                                                                                                  | -             |
| 30    | RW   | P3_INGRESS_CTRL             | P3 Ingress Limit Control<br>1:ON<br>0:OFF                                                                                                                                                                                                                                                 | 0x0           |
| 29    | RW   | P3_MNG_PKT_BY<br>PASS       | P3 Management Packet Bypass<br>Per packet dropped by ingress rate limit, the management frames can be ignored when the bit is set.<br>(Only bypass BPDUs, IGMP & MLD packets)<br>0: all packet included<br>1: Management Frame excluded                                                   | 0x0           |
| 28    | RW   | P3_INGRESS_FLO<br>W_CTRL_ON | Port 3 Ingress rate flow control<br>When the bit is set, the pause frame is used prior to packet dropped according to P3_ING_THRES. If the bucket is empty, then P3 will start to discard the received packets except those specific packet in P3_MNG_PKT_BYPASS mode.<br>0: OFF<br>1: ON | 0x0           |
| 27:26 | RW   | P3_TIMER_TICK               | Port 3 Timer Tick<br>0 : 512 us<br>1 : 128 us<br>2 : 32 us<br>3 : 8 us                                                                                                                                                                                                                    | 0x0           |
| 25:16 | RW   | P3_TOKEN                    | Port 3 Token<br>Every timer tick, Token number bytes will be added into the bucket. (Unit : Byte)<br>The maximum space of this bucket is 16'hFFFF bytes                                                                                                                                   | 0x0           |
| 15    | -    | -                           | Reserved                                                                                                                                                                                                                                                                                  | -             |

|       |    |                         |                                                                                                                                                                                                                                                                                           |     |
|-------|----|-------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|
| 14    | RW | P2_INGRESS_CTRL         | P2 Ingress Limit Control<br>1:ON<br>0:OFF                                                                                                                                                                                                                                                 | 0x0 |
| 13    | RW | P2_MNG_PKT_BY<br>PASS   | P2 Management Packet Bypass<br>Per packet dropped by ingress rate limit, the management frames can be ignored when the bit is set.<br>(Only bypass BPDUs, IGMP & MLD packets)<br>0: all packet included<br>1: Management Frame excluded                                                   | 0x0 |
| 12    | RW | P2_INGRESS_FLOW_CTRL_ON | Port 2 Ingress rate flow control<br>When the bit is set, the pause frame is used prior to packet dropped according to P2_ING_THRES. If the bucket is empty, then P2 will start to discard the received packets except those specific packet in P2_MNG_PKT_BYPASS mode.<br>0: OFF<br>1: ON | 0x0 |
| 11:10 | RW | P2_TIMER_TICK           | Port 2 Timer Tick<br>0 : 512 us<br>1 : 128 us<br>2 : 32 us<br>3 : 8 us                                                                                                                                                                                                                    | 0x0 |
| 9:0   | RW | P2_TOKEN                | Port 2 Token<br>Every timer tick, Token number bytes will be added into the bucket. (Unit : Byte)<br>The maximum space of this bucket is 16'hFFFF bytes                                                                                                                                   | 0x0 |

**P45\_ING\_CTRL: Port 4 & 5 Ingress Rate Limit Control(offset: 0x0124)**

| Bits | Type | Name                    | Description                                                                                                                                                                                                                                                                                                                                                         | Initial value |
|------|------|-------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31   | -    | -                       | Reserved                                                                                                                                                                                                                                                                                                                                                            | -             |
| 30   | RW   | P5_INGRESS_CTRL         | P5 Ingress Limit Control<br>1:ON<br>0:OFF<br>(Note: This feature is only valid when port 5 Giga MAC is implemented)                                                                                                                                                                                                                                                 | 0x0           |
| 29   | RW   | P5_MNG_PKT_BY<br>PASS   | P5 Management Packet Bypass<br>Per packet dropped by ingress rate limit, the management frames can be ignored when the bit is set.<br>(Only bypass BPDUs, IGMP & MLD packets)<br>0: all packet included<br>1: Management Frame excluded<br>(Note: This feature is only valid when port 5 Giga MAC is implemented)                                                   | 0x0           |
| 28   | RW   | P5_INGRESS_FLOW_CTRL_ON | Port 5 Ingress rate flow control<br>When the bit is set, the pause frame is used prior to packet dropped according to P5_ING_THRES. If the bucket is empty, then P5 will start to discard the received packets except those specific packet in P5_MNG_PKT_BYPASS mode.<br>0: OFF<br>1: ON<br>(Note: This feature is only valid when port 5 Giga MAC is implemented) | 0x0           |

|       |    |                         |                                                                                                                                                                                                                                                                                           |     |
|-------|----|-------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|
| 27:26 | RW | P5_TIMER_TICK           | Port 5 Timer Tick<br>0 : 512 us<br>1 : 128 us<br>2 : 32 us<br>3 : 8 us<br>(Note: This feature is only valid when port 5 Giga MAC is implemented)                                                                                                                                          | 0x0 |
| 25:16 | RW | P5_TOKEN                | Port 5 Token<br>Every timer tick, Token number bytes will be added into the bucket. (Unit : Byte)<br>The maximum space of this bucket is 16'hFFFF bytes<br>(Note: This feature is only valid when port 5 Giga MAC is implemented)                                                         | 0x0 |
| 15    | -  | -                       | Reserved                                                                                                                                                                                                                                                                                  | -   |
| 14    | RW | P4_INGRESS_CTRL         | P4 Ingress Limit Control<br>1:ON<br>0:OFF                                                                                                                                                                                                                                                 | 0x0 |
| 13    | RW | P4_MNG_PKT_BYPASS       | P4 Management Packet Bypass<br>Per packet dropped by ingress rate limit, the management frames can be ignored when the bit is set.<br>(Only bypass BPDU, IGMP & MLD packets)<br>0: all packet included<br>1: Management Frame excluded ets)                                               | 0x0 |
| 12    | RW | P4_INGRESS_FLOW_CTRL_ON | Port 4 Ingress rate flow control<br>When the bit is set, the pause frame is used prior to packet dropped according to P4_ING_THRES. If the bucket is empty, then P4 will start to discard the received packets except those specific packet in P4_MNG_PKT_BYPASS mode.<br>0: OFF<br>1: ON | 0x0 |
| 11:10 | RW | P4_TIMER_TICK           | Port 4 Timer Tick<br>0 : 512 us<br>1 : 128 us<br>2 : 32 us<br>3 : 8 us                                                                                                                                                                                                                    | 0x0 |
| 9:0   | RW | P4_TOKEN                | Port 4 Token<br>Every timer tick, Token number bytes will be added into the bucket. (Unit : Byte)<br>The maximum space of this bucket is 16'hFFFF bytes                                                                                                                                   | 0x0 |

**P0\_ING\_THRES: Port 0 Ingress Rate Limit Threshold(offset: 0x0128)**

| Bits  | Type | Name                   | Description                                                                                                                                                                                          | Initial value |
|-------|------|------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:16 | RW   | P0_IN_FC_OFF_THRESHOLD | Port 0 ingress rate limit flow control off.<br>If P0_INGRESS_FLOW_CTRL_ON = 1 and P0 Flow control capability is on (XFC status in 0x80), then P0 will initiate PAUSE OFF frame or stop backpressure. | 0xaaaa        |
| 15:0  | RW   | P0_IN_FCON_THRESH      | Port 0 ingress rate limit flow control on.<br>If P0_INGRESS_FLOW_CTRL_ON = 1 and P0 Flow control capability is on (XFC status in 0x80), then P0 will initiate PAUSE ON frame or backpressure.        | 0x5555        |

**P1\_ING\_THRES: Port 1 Ingress Rate Limit Threshold(offset: 0x012c)**

| Bits  | Type | Name                    | Description                                 | Initial value |
|-------|------|-------------------------|---------------------------------------------|---------------|
| 31:16 | RW   | P1_IN_FC_OFF_TH RESHOLD | Port 1 ingress rate limit flow control off. | 0xaaaa        |
| 15:0  | RW   | P1_IN_FCON_THR ES       | Port 1 ingress rate limit flow control on.  | 0x5555        |

**P2\_ING\_THRES: Port 2 Ingress Rate Limit Threshold(offset: 0x0130)**

| Bits  | Type | Name                    | Description                                 | Initial value |
|-------|------|-------------------------|---------------------------------------------|---------------|
| 31:16 | RW   | P2_IN_FC_OFF_TH RESHOLD | Port 2 ingress rate limit flow control off. | 0xaaaa        |
| 15:0  | RW   | P2_IN_FCON_THR ES       | Port 2 ingress rate limit flow control on.  | 0x5555        |

**P3\_ING\_THRES: Port 3 Ingress Rate Limit Threshold(offset: 0x0134)**

| Bits  | Type | Name                    | Description                                 | Initial value |
|-------|------|-------------------------|---------------------------------------------|---------------|
| 31:16 | RW   | P3_IN_FC_OFF_TH RESHOLD | Port 3 ingress rate limit flow control off. | 0xaaaa        |
| 15:0  | RW   | P3_IN_FCON_THR ES       | Port 3 ingress rate limit flow control on.  | 0x5555        |

**P4\_ING\_THRES: Port 4 Ingress Rate Limit Threshold(offset: 0x0138)**

| Bits  | Type | Name                    | Description                                 | Initial value |
|-------|------|-------------------------|---------------------------------------------|---------------|
| 31:16 | RW   | P4_IN_FC_OFF_TH RESHOLD | Port 4 ingress rate limit flow control off. | 0xaaaa        |
| 15:0  | RW   | P4_IN_FCON_THR ES       | Port 4 ingress rate limit flow control on.  | 0x5555        |

**P5\_ING\_THRES: Port 5 Ingress Rate Limit Threshold(offset: 0x013c)**

| Bits  | Type | Name                    | Description                                                                                                           | Initial value |
|-------|------|-------------------------|-----------------------------------------------------------------------------------------------------------------------|---------------|
| 31:16 | RW   | P5_IN_FC_OFF_TH RESHOLD | Port 5 ingress rate limit flow control off.<br>(Note: This feature is only valid when port 5 Giga MAC is implemented) | 0xaaaa        |
| 15:0  | RW   | P5_IN_FCON_THR ES       | Port 5 ingress rate limit flow control on.<br>(Note: This feature is only valid when port 5 Giga MAC is implemented)  | 0x5555        |

**P01\_EG\_CTRL: Port 0 & 1 Egress Rate Limit Control(offset: 0x0140)**

| Bits  | Type | Name           | Description                                                                                                                                                    | Initial value |
|-------|------|----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:29 | -    | -              | Reserved                                                                                                                                                       | -             |
| 28    | RW   | P1_EGRESS_CTRL | Port 1 Egress Control<br>1:ON<br>0:OFF                                                                                                                         | 0x0           |
| 27:26 | RW   | P1_TIMER_TICK  | Port 1 Timer Tick<br>0 : 512 us<br>1 : 128 us<br>2 : 32 us<br>3 : 8 us                                                                                         | 0x0           |
| 25:16 | RW   | P1_TOKEN       | Port 1 Token<br>Every timer tick, Token number bytes will be added into the egress bucket. (Unit : Byte)<br>The maximum space of this bucket is 16'hFFFF bytes | 0x0           |

|       |    |                |                                                                                                                                                                |     |
|-------|----|----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|
| 15:13 | -  | -              | Reserved                                                                                                                                                       | 0x0 |
| 12    | RW | PO_EGRESS_CTRL | Port 0 Egress Control<br>1:ON<br>0:OFF                                                                                                                         | 0x0 |
| 11:10 | RW | PO_TIMER_TICK  | Port 0 Timer Tick<br>0 : 512 us<br>1 : 128 us<br>2 : 32 us<br>3 : 8 us                                                                                         | 0x0 |
| 9:0   | RW | PO_TOKEN       | Port 0 Token<br>Every timer tick, Token number bytes will be added into the egress bucket. (Unit : Byte)<br>The maximum space of this bucket is 16'hFFFF bytes | 0x0 |

**P23\_EG\_CTRL: Port 2 & 3 Egress Rate Limit Control(offset: 0x0144)**

| Bits  | Type | Name           | Description                                                                                                                                                    | Initial value |
|-------|------|----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:29 | -    | -              | Reserved                                                                                                                                                       | -             |
| 28    | RW   | P3_EGRESS_CTRL | Port 3 Egress Control<br>1:ON<br>0:OFF                                                                                                                         | 0x0           |
| 27:26 | RW   | P3_TIMER_TICK  | Port 3 Timer Tick<br>0 : 512 us<br>1 : 128 us<br>2 : 32 us<br>3 : 8 us                                                                                         | 0x0           |
| 25:16 | RW   | P3_TOKEN       | Port 3 Token<br>Every timer tick, Token number bytes will be added into the egress bucket. (Unit : Byte)<br>The maximum space of this bucket is 16'hFFFF bytes | 0x0           |
| 15:13 | -    | -              | Reserved                                                                                                                                                       | -             |
| 12    | RW   | P2_EGRESS_CTRL | Port 2 Egress Control<br>1:ON<br>0:OFF                                                                                                                         | 0x0           |
| 11:10 | RW   | P2_TIMER_TICK  | Port 2 Timer Tick<br>0 : 512 us<br>1 : 128 us<br>2 : 32 us<br>3 : 8 us                                                                                         | 0x0           |
| 9:0   | RW   | P2_TOKEN       | Port 2 Token<br>Every timer tick, Token number bytes will be added into the egress bucket. (Unit : Byte)<br>The maximum space of this bucket is 16'hFFFF bytes | 0x0           |

**P45\_EG\_CTRL: Port 4 & 5 Egress Rate Limit Control(offset: 0x0148)**

| Bits  | Type | Name           | Description                                                                                                      | Initial value |
|-------|------|----------------|------------------------------------------------------------------------------------------------------------------|---------------|
| 31:29 | -    | -              | Reserved                                                                                                         | -             |
| 28    | RW   | P5_EGRESS_CTRL | Port 5 Egress Control<br>1:ON<br>0:OFF<br>(Note: This feature is only valid when port 5 Giga MAC is implemented) | 0x0           |

|       |    |                |                                                                                                                                                                                                                                          |     |
|-------|----|----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|
| 27:26 | RW | P5_TIMER_TICK  | Port 5 Timer Tick<br>0 : 512 us<br>1 : 128 us<br>2 : 32 us<br>3 : 8 us<br>(Note: This feature is only valid when port 5 Giga MAC is implemented)                                                                                         | 0x0 |
| 25:16 | RW | P5_TOKEN       | Port 5 Token<br>Every timer tick, Token number bytes will be added into the egress bucket. (Unit : Byte)<br>The maximum space of this bucket is 16'hFFFF bytes<br>(Note: This feature is only valid when port 5 Giga MAC is implemented) | 0x0 |
| 15:13 | -  | -              | Reserved                                                                                                                                                                                                                                 | -   |
| 12    | RW | P4_EGRESS_CTRL | Port 4 Egress Control<br>1:ON<br>0:OFF                                                                                                                                                                                                   | 0x0 |
| 11:10 | RW | P4_TIMER_TICK  | Port 4 Timer Tick<br>0 : 512 us<br>1 : 128 us<br>2 : 32 us<br>3 : 8 us                                                                                                                                                                   | 0x0 |
| 9:0   | RW | P4_TOKEN       | Port 4 Token<br>Every timer tick, Token number bytes will be added into the egress bucket. (Unit : Byte)<br>The maximum space of this bucket is 16'hFFFF bytes                                                                           | 0x0 |

**PCRI: Packet Counter Recycle Indication (offset: 0x014c)**

| Bits  | Type | Name         | Description                                                                                                                                                             | Initial value |
|-------|------|--------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31    | RW   | PTK_CNT_CLR  | Tx/Rx Packet Counters Write one Clear<br>When this bit is set, all Tx/Rx packet counters will be clear. This bit can be self-clear automatically.                       | 0x0           |
| 30    | -    | -            | Reserved                                                                                                                                                                | -             |
| 29:24 | W1C  | TCOL_PKT_REC | Per Port Transmitted Collision Packet Counter Recycle<br>This bit indicates that the per port transmitted collision packet counter recycles the count. Write one clear. | 0x0           |
| 23:22 | -    | -            | Reserved                                                                                                                                                                | -             |
| 22:16 | W1C  | TXOK_PKT_REC | Per Port Transmitted Good Packet Counter Recycle<br>This bit indicates that the per port transmitted good packet counter recycles the count. Write one clear.           | 0x0           |
| 15:14 | -    | -            | Reserved                                                                                                                                                                | -             |
| 13:8  | W1C  | BADD_PKT_REC | Per Port Received Bad Packet Counter Recycle<br>This bit indicates that the per port received bad packet counter recycles the count. Write one clear.                   | 0x0           |
| 8:7   | -    | -            | Reserved                                                                                                                                                                | -             |
| 6:0   | W1C  | GOOD_PKT_REC | Per Port Received Good Packet Counter Recycle<br>This bit indicates that the per port received good packet counter recycles the count. Write one clear.                 | 0x0           |

**POTPC: Port 0 TX Packet Counter (offset: 0x0150)**

| Bits | Type | Name | Description | Initial value |
|------|------|------|-------------|---------------|
|------|------|------|-------------|---------------|

|       |    |               |                                                            |     |
|-------|----|---------------|------------------------------------------------------------|-----|
| 31:16 | RO | BAD_PKT_CNT0  | Port 0 packet count for transmitted packets with collision | 0x0 |
| 15:0  | RO | GOOD_PKT_CNT0 | Port 0 packet counter for transmitted packets successfully | 0x0 |

**P1TPC: Port 1 TX Packet Counter (offset: 0x0154)**

| Bits  | Type | Name          | Description                                                | Initial value |
|-------|------|---------------|------------------------------------------------------------|---------------|
| 31:16 | RO   | BAD_PKT_CNT1  | Port 1 packet count for transmitted packets with collision | 0x0           |
| 15:0  | RO   | GOOD_PKT_CNT1 | Port 1 packet counter for transmitted packets successfully | 0x0           |

**P2TPC: Port 2 Packet Counter (offset: 0x0158)**

| Bits  | Type | Name          | Description                                                | Initial value |
|-------|------|---------------|------------------------------------------------------------|---------------|
| 31:16 | RO   | BAD_PKT_CNT2  | Port 2 packet count for transmitted packets with collision | 0x0           |
| 15:0  | RO   | GOOD_PKT_CNT2 | Port 2 packet counter for transmitted packets successfully | 0x0           |

**P3TPC: Port 3 TX Packet Counter (offset: 0x015c)**

| Bits  | Type | Name          | Description                                                | Initial value |
|-------|------|---------------|------------------------------------------------------------|---------------|
| 31:16 | RO   | BAD_PKT_CNT3  | Port 3 packet count for transmitted packets with collision | 0x0           |
| 15:0  | RO   | GOOD_PKT_CNT3 | Port 3 packet counter for transmitted packets successfully | 0x0           |

**P4TPC: Port 4 TX packet counter (offset: 0x0160)**

| Bits  | Type | Name          | Description                                                | Initial value |
|-------|------|---------------|------------------------------------------------------------|---------------|
| 31:16 | RO   | BAD_PKT_CNT4  | Port 4 packet count for transmitted packets with collision | 0x0           |
| 15:0  | RO   | GOOD_PKT_CNT4 | Port 4 packet counter for transmitted packets successfully | 0x0           |

**P5TPC: Port 5 TX packet counter (offset: 0x0164)**

| Bits  | Type | Name          | Description                                                                                                                          | Initial value |
|-------|------|---------------|--------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:16 | RO   | BAD_PKT_CNT4  | Port 5 packet count for transmitted packets with collision<br>(Note: This feature is only valid when port 5 Giga MAC is implemented) | 0x0           |
| 15:0  | RO   | GOOD_PKT_CNT4 | Port 5 packet counter for transmitted packets successfully<br>(Note: This feature is only valid when port 5 Giga MAC is implemented) | 0x0           |

**LEDC: LED Control Register (offset: 0x0168)**

| Bits | Type | Name         | Description                                                            | Initial value |
|------|------|--------------|------------------------------------------------------------------------|---------------|
| 31:5 | -    | RES          | Reserved                                                               | 0x0           |
| 4:0  | RW   | LED_POLARITY | Per PORT LED Polarity Control<br>1'b0: Low active<br>1'b1: High active | 0x0           |

### 3.20.5 MII control register

These registers could be accessed by PCR0 (PHY Control Register 0) and PCR1 indirectly. Among them, PHY reg0~1 and 4~6 are unique for each port. PHY reg2~3 are common for all 5 ports.

Legend:

SC: Self-clearing, RC: Read-clearing

LL: Latching Low, LH: Latching High

R/W: Read/write, RO: Read-Only

CR Address:00(d00) Reset State:3100

| Bit | Read/Write | Name                   | Description                                                     | Default |
|-----|------------|------------------------|-----------------------------------------------------------------|---------|
| 15  | RW; SC     | MR_MAIN_RESET          | 1=Reset: 0=Normal, reset all digital logic, except phy_reg      | 0x0     |
| 14  | RW         | LOOPBACK_MII           | Mii loop back                                                   | 0x0     |
| 13  | RW         | FORCE_SPEED            | 1 = 100Mbps: 0=10Mbps, when mr_autoneg_enable = 1'b0            | 0x1     |
| 12  | RW         | MR_AUTONEG_ENABLE      | 1= Enabled: 0=Normal                                            | 0x1     |
| 11  | RW         | POWERDOWN              | phy into power down (power down analog TX analog RX, analog AD) | 0x0     |
| 10  | -          | -                      | Reserved                                                        | 0x0     |
| 9   | RW; SC     | MR_RESTART_NEGOTIATION | 1 = Restart Auto-Negotiation: 0 = Normal                        | 0x0     |
| 8   | RW         | FORCE_DUPLEX           | 1 = Full Duplex: 0 = Half Duplex, when mr_autoneg_enable = 1'b0 | 0x1     |
| 7:0 | -          | -                      | Reserved                                                        | 0x0     |

MII status register

CR Address:01(d01) Reset State: 7849

| Bit | Read/Write | Name                    | Description                                                                                                    | Default |
|-----|------------|-------------------------|----------------------------------------------------------------------------------------------------------------|---------|
| 15  | -          | 100 BASE T4             | Not supported                                                                                                  | 0x0     |
| 14  | RO         | 100BASE-X Full Duplex   | 1 = PHY is 100BASE-X full duplex capable<br>0 = PHY is not 100BASE-X full duplex capable                       | 0x1     |
| 13  | RO         | 100BASE-X Half Duplex   | 1 = PHY is 100BASE-X half duplex capable<br>0 = PHY is not 100BASE-X half duplex capable                       | 0x1     |
| 12  | RO         | 10Mbps/s Full Duplex    | 1 = PHY is 10Mbps/s Full duplex capable<br>0 = PHY is not 10Mbps/s Full duplex capable                         | 0x1     |
| 11  | RO         | 10 Mb/s Half Duplex     | 1 = PHY is 10Mbps/s Half duplex capable<br>0 = PHY is not 10Mbps/s Half duplex capable                         | 0x1     |
| 10  | RO         | 100BASE-T2 full duplex  | Not supported                                                                                                  | 0x0     |
| 9   | RO         | 100BASE-T2 half duplex  | Not supported                                                                                                  | 0x0     |
| 8:7 | -          | -                       | Reserved                                                                                                       | -       |
| 6   | RO         | MF Preamble Suppression | 1 = PHY can accept management frames with preamble suppression<br>0 = PHY cannot accept management frames with | 0x1     |



|   |           |                     |                                                                             |     |
|---|-----------|---------------------|-----------------------------------------------------------------------------|-----|
|   |           |                     | preamble suppression                                                        |     |
| 5 | RO        | mr_autoneg_complete | 1 = auto-negotiate completed,<br>0 = auto-negotiate incomplete              | 0x0 |
| 4 | -         | -                   | Reserved                                                                    | -   |
| 3 | RO        | Autoneg Ability     | 1 = PHY can auto-negotiate,<br>0 = PHY cannot auto-negotiate                | 0x1 |
| 2 | RO/LL     | Link Status         | 1 = link is up,<br>0 = link is down                                         | 0x0 |
| 1 | RO/LH; RC | Jabber Detect       | 1 = jabber condition detected                                               | 0x0 |
| 0 | RO        | Extended Capability | 1=extended register capabilities,<br>0=basic register set capabilities only | 0x1 |

#### PHY identifier register

CR Address:02(d02) Reset State: 00c3

| Bit  | Read/Write | Name          | Description                         | Default |
|------|------------|---------------|-------------------------------------|---------|
| 15:0 | RO         | PHY_ID[31-16] | OUI (bits 3-18). Ralink OUI =000C43 | 0xc3    |

#### PHY version register

CR Address:03(d03) Reset State: 0800

| Bit   | Read/Write | Name          | Description                                                                 | Default |
|-------|------------|---------------|-----------------------------------------------------------------------------|---------|
| 15:10 | RO         | PHY_ID[15-10] | OUI (bits 19-24)                                                            | 0x2     |
| 9:4   | RO         | PHY_ID[9-4]   | Manufacturer's Model Number (bits 5-0)                                      | 0x0     |
| 3:0   | RO         | PHY_ID[3-0]   | Revision Number (bits3-0);<br>Register 3, bit 0 is LS bit of PHY Identifier | 0x0     |

#### Auto-Negotiation advertisement register

CR Address:04(d04) Reset State: 05e1

| Bit   | Read/Write | Name                            | Description                                                | Default |
|-------|------------|---------------------------------|------------------------------------------------------------|---------|
| 15    | RO         | Next Page Enable                | 1=Set to use Next Page: 0=Not to use Next Page             | 0x0     |
| 14    | -          | -                               | Reserved                                                   | 0x0     |
| 13    | RW         | Remote Fault Enable             | 1 = Auto Negotiation Fault Detected<br>0 = No Remote Fault | 0x0     |
| 12:11 | RO         | Not Implemented                 | Technology Ability A7-A6                                   | 0x0     |
| 10    | RW         | Pause                           | Technology Ability A5                                      | 0x1     |
| 9     | RO         | Not Implemented                 | Technology Ability A4                                      | 0x0     |
| 8     | RW         | 100Base-TX Full Duplex Capable  | 1 = Capable of Full Duplex<br>0 = Not Capable              | 0x1     |
| 7     | RW         | 100 Base-TX Half Duplex Capable | 1 = Capable of Half Duplex<br>0 = Not Capable              | 0x1     |
| 6     | RW         | 10 Base-T Full Duplex Capable   | 1 = Capable of Full Duplex 10BASE-T<br>0 = Not Capable     | 0x1     |
| 5     | RW         | 10 Base-T Half Duplex Capable   | 1 = Capable of Half Duplex 10BASE-T<br>0 = Not Capable     | 0x1     |
| 4:0   | RW         | Selector Field                  | Identifies type of message                                 | 0x1     |

#### Auto-Negotiation Link partner (LP) ability register

CR Address:05(d05) Reset State: 0000

| Bit | Read/Write | Name | Description | Default |
|-----|------------|------|-------------|---------|
|-----|------------|------|-------------|---------|

|           |     |                                 |                                                                              |     |
|-----------|-----|---------------------------------|------------------------------------------------------------------------------|-----|
| 15        | R O | Next Page                       | 1=Link Partner is requesting Next Page function<br>0=Base Page is requested. | 0x0 |
| 14        | R O | Acknowledge                     | 1= Link partner acknowledge Received Successfully<br>0 =Not Received         | 0x0 |
| 13        | R O | Remote Fault                    | 1 = Auto Negotiation Fault Detected<br>0 = No Remote Fault                   | 0x0 |
| 12:1<br>1 | R O | Not implemented                 | Technology Ability A7-A6                                                     | 0x0 |
| 10        | R O | Pause                           | Technology Ability A5                                                        | 0x0 |
| 9         | R O | Not Implemented                 | Technology Ability A4                                                        | 0x0 |
| 8         | R O | 100Base-TX Full Duplex Capable  | 1 = Capable<br>0 = Not Capable                                               | 0x0 |
| 7         | R O | 100 Base-TX Half Duplex Capable | 1 = Capable<br>0 = Not Capable                                               | 0x0 |
| 6         | R O | 10 Base-T Full Duplex Capable   | 1 = Capable<br>0 = Not Capable                                               | 0x0 |
| 5         | R O | 10 Base-T Half Duplex Capable   | 1 = Capable<br>0 = Not Capable                                               | 0x0 |
| 4:0       | RO  | Selector Field                  | Identifies type of message                                                   | 0x0 |

Auto-Negotiation expansion register

CR Address:06(d06) Reset State: 0000

| Bit  | R/W/Type  | Name                               | Description                                                                                | Default |
|------|-----------|------------------------------------|--------------------------------------------------------------------------------------------|---------|
| 15:5 | -         | -                                  | Reserved                                                                                   | -       |
| 4    | RO/LH; RC | Parallel Detection Fault           | 1 = Local Device Parallel Detection Fault<br>0 = No fault detected                         | 0x0     |
| 3    | RO        | Link Partner Next Page Able        | 1 = Link Partner is Next Page Able<br>0 = Link Partner is not Next Page Able               | 0x0     |
| 2    | RO        | mr_np_able                         | 1 = Local device is Next Page Able<br>0 = Local device is not Next Page Able               | 0x0     |
| 1    | RO/LH; RC | Page Received                      | 1 = A New Page has been received<br>0 = A New Page has not been received                   | 0x0     |
| 0    | RO        | Link Partner Auto-negotiation Able | 1 = Link Partner is Auto-negotiation able<br>0 = Link Partner is not Auto-negotiation able | 0x0     |

### 3.20.6 Function Description

#### 3.20.6.1 Flow control settings

For both FE or GE ports, flow control enable/disable is decided by :

1. Force mode is the highest priority,
  - 1.1 GE ports use FPA : Force Port 5 ~Port 6 ability (offset:0xC8)
    - [11:10] Enable port6 or 5 force mode
    - [9:8] Port 6 flow control ability ( Support asymmetric flow control [9]:TX [8]:RX)
    - [7:6] Port 5 flow control ability
  - 1.2 FE ports use FPA: Force Port4 ~ Port0 Ability (offset: 0x84)
    - [31:27] Enable port 4 ~ 0 force mode
    - [26:22] Port 4 ~ 0 flow control ability (Only support symmetric flow control)
2. If the force mode is disabled, then use the flow control status after auto-negotiation.  
 But there is one exception for flow control : when POC1: Port Control 0 (offset: 0x90) [14:8] "EN\_FC "pause flow control is disabled, then flow control will be disabled without regard to the AN result.  
 (For GE ports, Port5 or 6, EN\_FC[port\_num] = 0 will disable both TX and RX flow control)  
  
 No matter using force or AN mode, the final flow control enable/disable value will show on POA: Port Ability (offset: 0x80) [24:16] for port 0 ~ 6
3. Another exception on PFC0: Priority flow control – 0 (offset: 0x10) [23:16] Turn off flow control, For Q3 traffic, the user can use this register to turn off the flow control.

#### 3.20.6.2 VID and Tagging

##### 3.20.6.2.1 VID and VLAN member set

RT5350 supports 16 VLANs. It can be configured to identify any 16 out of 4096 possible VIDs. These 16 VIDs could be configured by setting VIDx (X=0~15) registers. To configure the member set ports of a given VLAN, one can set the VLAN\_MEMSET\_x (x=0~15) register. Each bit of the VLAN\_MEMSET\_x register is corresponding to the associated port. For example, to configure port #1 and port #3 as the member ports of VLAN 5, one can set VLAN\_MEMSET\_5 as 8'b00001010.

##### 3.20.6.2.2 Tag and Untag

There is a per port register to configure the egress tag and untag setting. If one does not want VLAN tagged frame transmitted from a given port x, he could set UNTAG\_EN[x]=1; If one wants VLAN tagged frame transmitted from port y, he could set UNTAG\_EN[y]=0. RT5350 supports VLAN tag/untag by per egress port basis. It does not support per VLAN per port basis.

##### 3.20.6.2.3 Port VID

There is per port Px\_PVID register to support PVID. The Px\_PVID is assigned to a incoming frame which is untagged or priority tagged (i.e. VID filed =0).

##### 3.20.6.2.4 Double Tag

RT5350 supports double VLAN tags by setting a per ingress port register – DOUBLE\_TAG\_EN[x]. When RT5350 receives a frame from a port with DOUBLE\_TAG\_EN = 1, it will ignore the VLAN tag filed, if any, and insert the associated PVID in front of the frame after the MAC SA field. Then,

it will go on the frame forwarding decision based on this PVID. When this frame is finally be transmitted to an egress port with UNTAG\_EN=0, the egress packet will be double VLAN tagged if its incoming format is single VLAN tag; it will be single VLAN tagged if its incoming format is non-VLAN tagged. Please see the following figure for some examples.

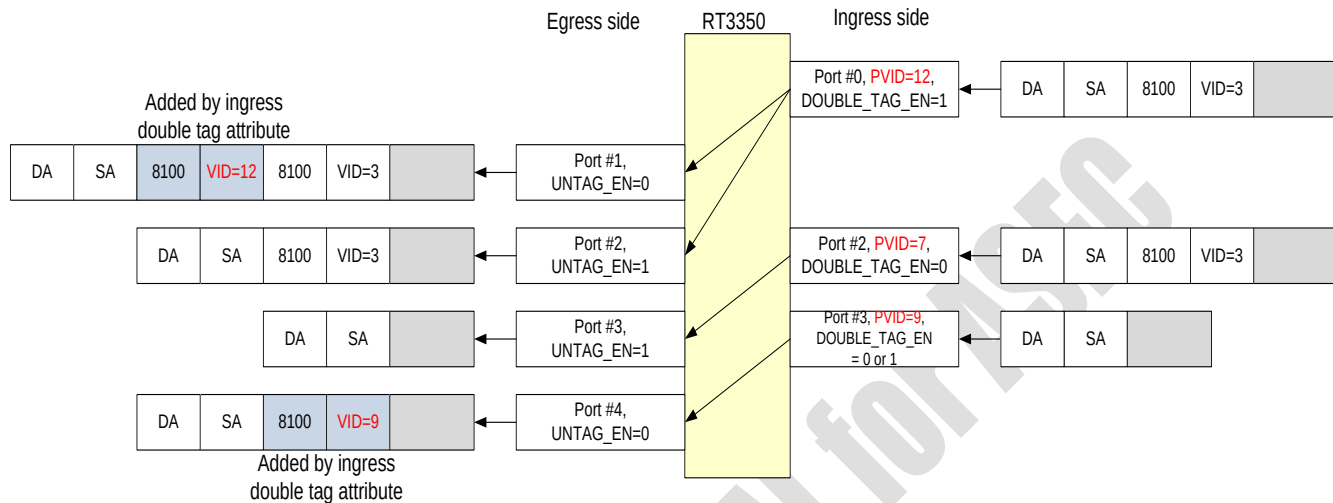


Fig. 3-18-2 Double Tag

### 3.20.6.2.5 Special Tag

In order to let the recipient (e.g. RT5350 internal CPU or external 3rd party CPU) knows the incoming port number of a received frame, a special tag is supported to rewrite the TPID (0x8100) filed with the incoming port number. The format of this rewritten TPID is : 810x, where x specifies the incoming port number. To enable this feature, one should set CPU\_TPID\_EN=1 first and specify output ports that need incoming port number to be carried by TPID by setting the associated ports in TX\_CPU\_TPID\_BIT\_MAP[6:0]. Please be noted, this special tag feature is a supplement to the existing VLAN tag feature. If the egress frame does not have VLAN tag, there is no way for RT5350 to put incoming port number into the modified TPID field. If the egress frame is double VLAN tagged, the special tag applies to the outer VLNA tag only. Please see the following figure for some examples.

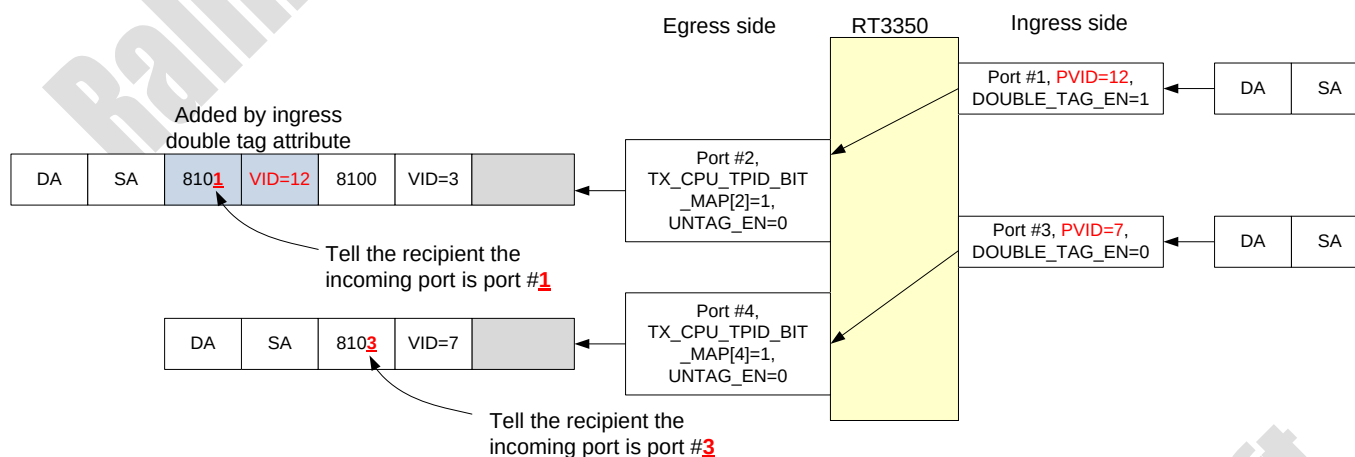


Fig. 3-18-3 Special Tag

### 3.20.6.3 Packet Classification, QoS, Scheduling and Buffer control

RT5350 supports 4 CoS queues per egress port. When a frame is received, it is classified by IP DSCP, 802.1p tag and incoming port priority. The classify sequence is 802.1p tag first, then IP DSCP, and finally the incoming port priority. To enable IP DSCP classification for port x, one has to set EN\_TOS[x] to 1; To enable 802.1p tag classification for port x, one has to set EN\_VLAN[x] to 1. If both EN\_TOS[x] and EN\_VLAN[x] are zero or could not be applied (for non-IP or non-VLAN frames), frame will be classified by the PORT\_PRIx register. The IP DSCP and 802.1p user priority to CoS queue mapping are specified by the following tables :

| IP DSCP (decimal value) | CoS Queue Mapping |
|-------------------------|-------------------|
| 0~15                    | BK_q              |
| 16~31                   | BE_q              |
| 32~47                   | CL_q              |
| 48~63                   | VO_q              |

| 802.1p priority (decimal value) | CoS Queue Mapping |
|---------------------------------|-------------------|
| 1, 2                            | BK_q              |
| 0, 3                            | BE_q              |
| 4, 5                            | CL_q              |
| 6, 7                            | VO_q              |

At the egress side, there is a SP/WRR scheduler for each output port to schedule the frame transmission opportunity. One can assign the weight for each of the VO/CL/BE/BK queues to specify the service ratio. It also support a mixed schedule mode to treat VO queue as the strict priority by assigning its weight (VO\_NUM) to zero.

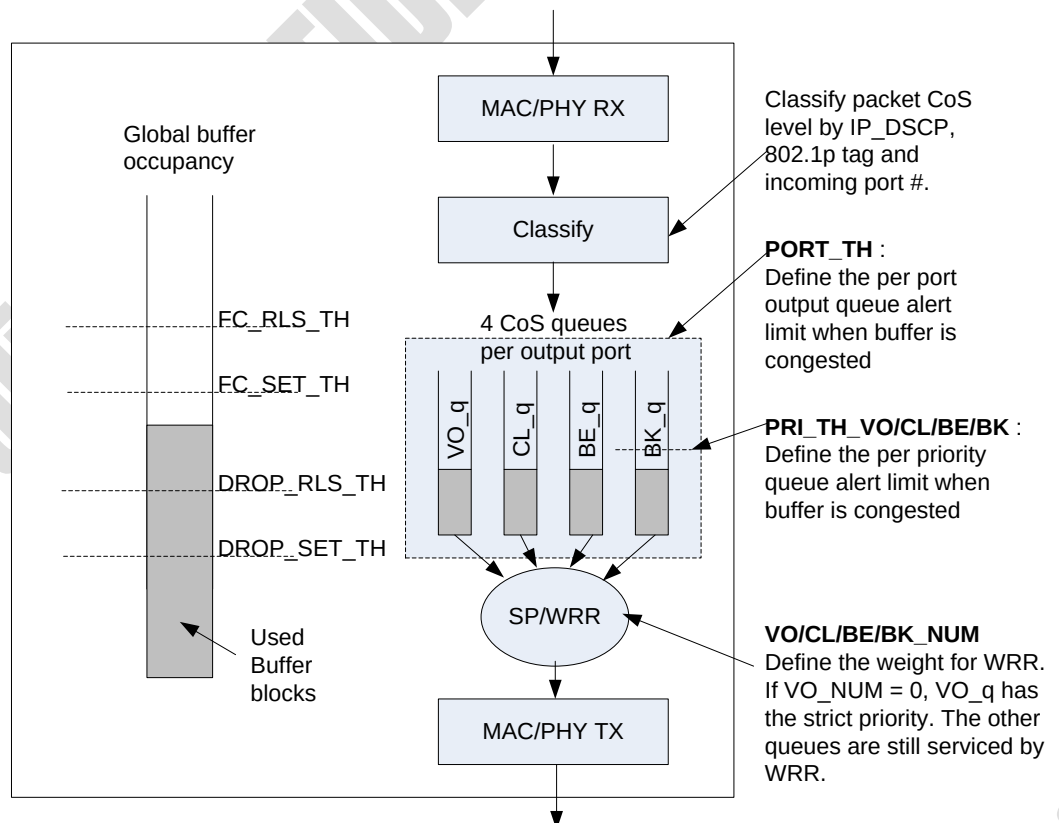


Fig. 3-18-4 Packet Classification, QoS, Scheduling and Buffer control

To support QoS-awared flow control, there is a global per CoS queue threshold setting to define the alert threshold when global packet buffer is getting congested. When the global buffer block count is lower than FC\_SET\_TH, an incoming frame will trigger a pause\_ON frame to be transmitted if the PORT\_TH of the destination port and PRI\_TH\_xx (xx = VO or CL or BE or BK) are both reached. By this sophisticated buffer control mechanism, the high priority traffic (e.g. VoIP) will not get dropped or paused if it is put in strict priority VO\_q and its source rate is controlled.

The above description for QoS-awared flow control could be worked even well if we turn on SW2FE\_WL\_FC\_EN (Switch to Frame Engine WAN-LAN flow control) for one-armed router application. Since there is only a single GE port connecting the frame engine and the embedded Ethernet switch, the traditional 802.3x pause mechanism might block all frames from CPU to the Ethernet switch regardless of frame's destination (LAN or WAN). In other words, there will be HOL (Head-of-Line) blocking in this one-armed router case. To relief the HOL, one could tell the Ethernet switch which ports are LAN ports by specifying the ports into LAN\_PMAP register. Together with separated LAN/WAN GDMA in the frame engine, a better QoS-awared flow control could be supported.

#### 3.20.6.4 Spanning Tree Protocol

To eliminate the LAN loop, Spanning Tree Protocol(STP) can be used to detect the loop and maintain the spanning tree topology. RT5350 can support different port states, frame forwarding and learning capability to meet the STP requirements. Below table expresses the relative port states and the corresponding capabilities.

| Port State | Receive BPDU | Transmit BPDU | Learn Address | Forward Frame |
|------------|--------------|---------------|---------------|---------------|
| Disabled   | -            | -             | -             | -             |
| Blocking   | V            | -             | -             | -             |
| Listening  | V            | V             | -             | -             |
| Learning   | V            | V             | V             | -             |
| Forwarding | V            | V             | V             | V             |

To emulate the different port behaviors, user can configure the following registers based on which port state the software will apply one port to.

##### 1. Disabled -

- Disable frame transmission(POC1.BLOCKING\_STATE=0x1)
- Not participate in the operation of the Spanning Tree Protocol (SGC.RMC\_RULE=0x2)
- Disable Source MAC Learning(POC1.DIS\_LRNING=0x1)

##### 2. Blocking -

- Disable frame transmission (POC1.BLOCKING\_STATE=0x1)
- Participate in the Spanning Tree Protocol (SGC.RMC\_RULE=0x1)
- Disable Source MAC Learning(POC1.DIS\_LRNING=0x1)

##### 3. Listening -

- Disable frame transmission (POC1.BLOCKING\_STATE=0x1)
- Participate in the operation of the Spanning Tree Protocol (SGC.RMC\_RULE=0x1)
- Disable Source MAC Learning(POC1.DIS\_LRNING=0x1)

##### 4. Learning -

- Discard frame transmission(POC1.BLOCKING\_STATE=0x1)
- Participate in the operation of the Spanning Tree Protocol (SGC.RMC\_RULE=0x1)
- Enable Source MAC Learning(POC1.DIS\_LRNING=0x0)

##### 5. Forwarding -

- Enable frame transmission (POC1.BLOCKING\_STATE=0x0)

- Participate in the operation of the Spanning Tree Protocol (SGC.RMC\_RULE=0x1)
- Enable Source MAC Learning(POC1.DIS\_LRNING=0x0)

### 3.21 802.11n 1T1R MAC/BBP

#### 3.21.1 Features

- 1x1modes
- 150MHz PHY Rate Support
- Legacy and High Throughput Modes
- 20MHz/40MHz bandwidth
- Reverse Direction Data Flow and Frame Aggregation
- WEP 64/128, WPA, WPA2,WAPI Support
- QoS – WMM, WMM-PS
- Wake on Wireless LAN
- 16-Multiple BSSID Support
- International Regulation - 802.11d + h
- Cisco CCX V1.0 V2.0 V3.0 Compliance
- Bluetooth Co-existence
- Low Power with Advanced Power Management

#### 3.21.2 Block Diagram

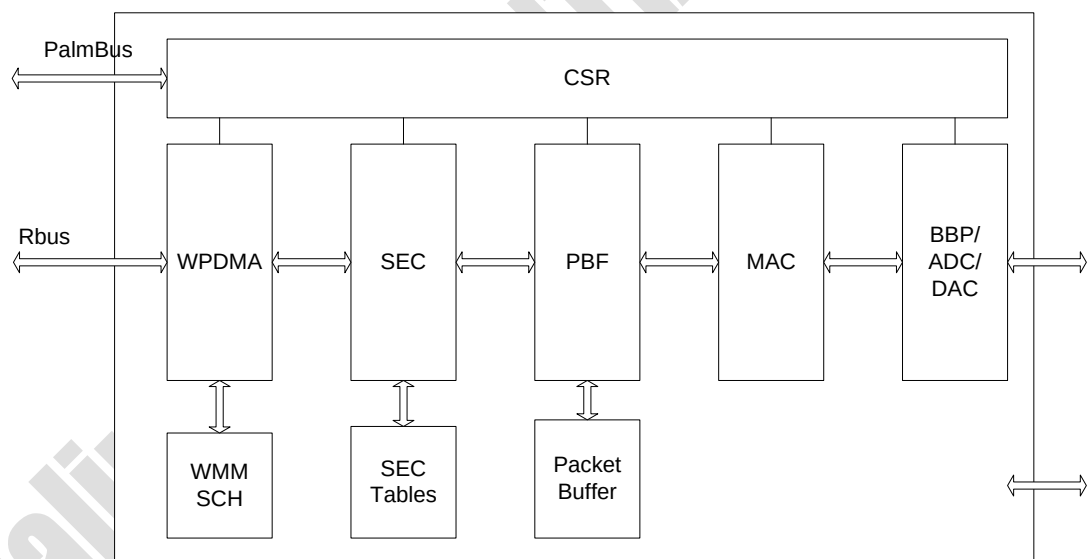


Fig. 5-17-1 802.11n 1T1R MAC/BBP block diagram



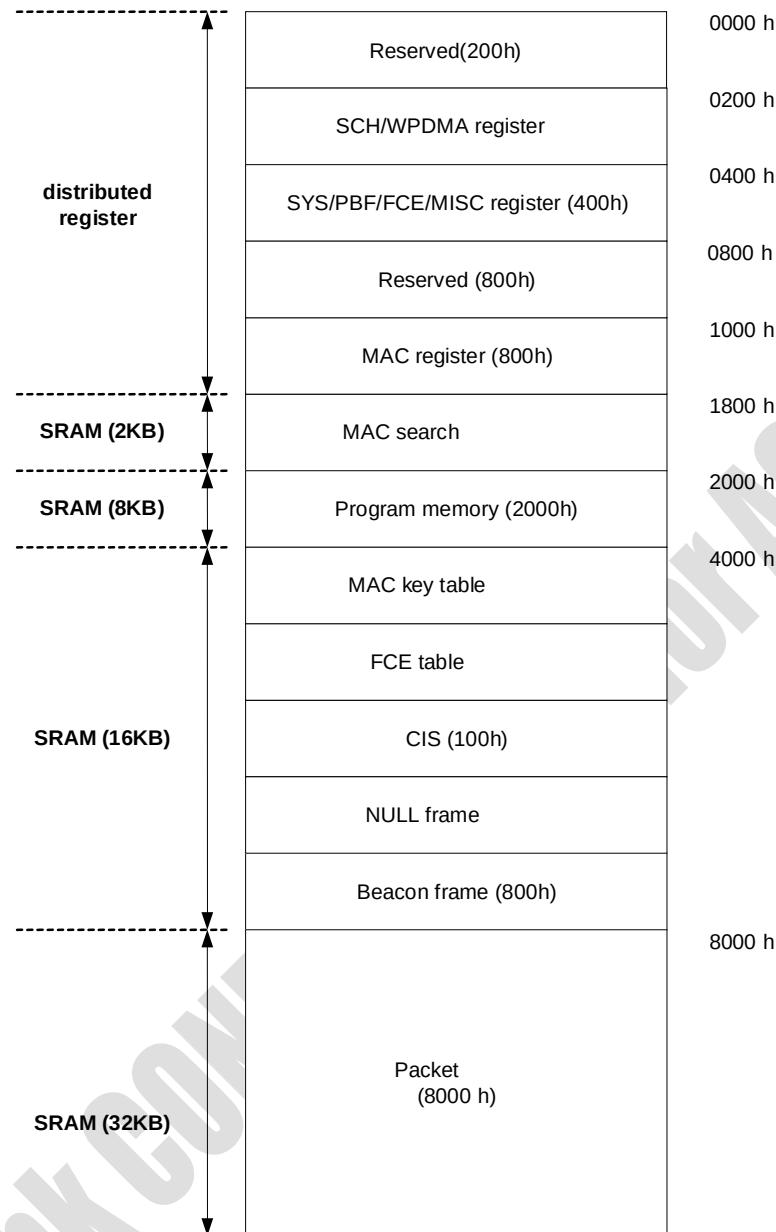


Fig. 5-17-2 802.11n 3T3R MAC/BBP register map

### 3.3.1 Register Description - SCH/WPDMA (base: 0x1018\_0000)

INT\_STATUS: (offset: 0x0200)

| Bits  | Type | Name        | Description                                                                                                                          | Initial value |
|-------|------|-------------|--------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:21 | -    | -           | Reserved                                                                                                                             | 0x0           |
| 20    | RW   | RADAR_INT   | BBP radar detection interrupt                                                                                                        | 0x0           |
| 19:18 | -    | -           | Reserved                                                                                                                             | 0x0           |
| 17    | RW   | TX_COHERENT | TX_DMA finds data coherent event when checking ddone bit.<br>Write 1 to clear the interrupt.<br>Read to get the raw interrupt status | 0x0           |
| 16    | RW   | RX_COHERENT | RX_DMA finds data coherent event when checking ddone bit.<br>Write 1 to clear the interrupt.<br>Read to get the raw interrupt status | 0x0           |
| 15    | RW   | MAC_INT_4   | MAC interrupt 4: GP timer interrupt                                                                                                  | 0x0           |

|    |    |                |                                                                                                                             |     |
|----|----|----------------|-----------------------------------------------------------------------------------------------------------------------------|-----|
| 14 | RW | MAC_INT_3      | MAC interrupt 3: Auto wakeup interrupt                                                                                      | 0x0 |
| 13 | RW | MAC_INT_2      | MAC interrupt 2: TX status interrupt                                                                                        | 0x0 |
| 12 | RW | MAC_INT_1      | MAC interrupt 1: Pre-TBTT interrupt                                                                                         | 0x0 |
| 11 | RW | MAC_INT_0      | MAC interrupt 0: TBTT interrupt                                                                                             | 0x0 |
| 10 | RO | TX_RX_COHERENT | When TX_COHERENT or RX_COHERENT is on, this bit is set                                                                      | 0x0 |
| 9  | RW | MCU_CMD_INT    | MCU command interrupt                                                                                                       | 0x0 |
| 8  | RW | TX_DONE_INT5   | TX Queue#5 packet transmit interrupt<br>Write 1 to clear the interrupt.                                                     | 0x0 |
| 7  | RW | TX_DONE_INT4   | TX Queue#4 packet transmit interrupt<br>Write 1 to clear the interrupt.<br>Read to get the raw interrupt status             | 0x0 |
| 6  | RW | TX_DONE_INT3   | TX Queue#3 packet transmit interrupt<br>Write 1 to clear the interrupt.<br>Read to get the raw interrupt status             | 0x0 |
| 5  | RW | TX_DONE_INT2   | TX Queue#2 packet transmit interrupt<br>Write 1 to clear the interrupt.<br>Read to get the raw interrupt status             | 0x0 |
| 4  | RW | TX_DONE_INT1   | TX Queue#1 packet transmit interrupt<br>Write 1 to clear the interrupt.<br>Read to get the raw interrupt status             | 0x0 |
| 3  | RW | TX_DONE_INT0   | TX Queue#0 packet transmit interrupt<br>Write 1 to clear the interrupt.<br>Read to get the raw interrupt status             | 0x0 |
| 2  | RW | RX_DONE_INT    | RX packet receive interrupt<br>Write 1 to clear the interrupt.<br>Read to get the raw interrupt status                      | 0x0 |
| 1  | RW | TX_DLY_INT     | Summary of the whole WPDMA TX related interrupts<br>Write 1 to clear the interrupt.<br>Read to get the raw interrupt status | 0x0 |
| 0  | RW | RX_DLY_INT     | Summary of the whole WPDMA RX related interrupts Write 1 to clear the interrupt.<br>Read to get the raw interrupt status    | 0x0 |

INT\_MASK: (offset: 0x0204)

| Bits  | Type | Name           | Description                                                                                      | Initial value |
|-------|------|----------------|--------------------------------------------------------------------------------------------------|---------------|
| 31:21 | -    | -              | Reserved                                                                                         | 0x0           |
| 20    | RW   | RADAR_INT_EN   | Enable for BBP radar detection interrupt<br>1: Enable the interrupt<br>0: Disable the interrupt  | 0x0           |
| 19:18 | -    | -              | Reserved                                                                                         | 0x0           |
| 17    | RW   | TX_COHERENT_EN | Enable for TX_DMA data coherent interrupt<br>1: Enable the interrupt<br>0: Disable the interrupt | 0x0           |
| 16    | RW   | RX_COHERENT_EN | Enable for RX_DMA data coherent interrupt<br>1: Enable the interrupt<br>0: Disable the interrupt | 0x0           |
| 14    | RW   | MAC_INT4_EN    | MAC interrupt 4: GP timer interrupt                                                              | 0x0           |
| 14    | RW   | MAC_INT3_EN    | MAC interrupt 3: Auto wakeup interrupt                                                           | 0x0           |
| 13    | RW   | MAC_INT2_EN    | MAC interrupt 2: TX status interrupt                                                             | 0x0           |
| 12    | RW   | MAC_INT1_EN    | MAC interrupt 1: Pre-TBTT interrupt                                                              | 0x0           |
| 11    | RW   | MAC_INT0_EN    | MAC interrupt 0: TBTT interrupt                                                                  | 0x0           |
| 10    | -    | -              | Reserved                                                                                         | 0x0           |

|   |    |                  |                                                                                                           |     |
|---|----|------------------|-----------------------------------------------------------------------------------------------------------|-----|
| 9 | RW | MCU_CMD_INT_MSK  | MCU command interrupt enable<br>1 : Enable the interrupt<br>0 : Disable the interrupt                     | 0x0 |
| 8 | RW | TX_DONE_INT_MSK5 | TX Queue#5 packet transmit interrupt<br>1 : Enable the interrupt<br>0 : Disable the interrupt             | 0x0 |
| 7 | RW | TX_DONE_INT_MSK4 | TX Queue#4 packet transmit interrupt<br>1 : Enable the interrupt<br>0 : Disable the interrupt             | 0x0 |
| 6 | RW | TX_DONE_INT_MSK3 | TX Queue#3 packet transmit interrupt<br>1 : Enable the interrupt<br>0 : Disable the interrupt             | 0x0 |
| 5 | RW | TX_DONE_INT_MSK2 | TX Queue#2 packet transmit interrupt<br>1 : Enable the interrupt<br>0 : Disable the interrupt             | 0x0 |
| 4 | RW | TX_DONE_INT_MSK1 | TX Queue#1 packet transmit interrupt<br>1 : Enable the interrupt<br>0 : Disable the interrupt             | 0x0 |
| 3 | RW | TX_DONE_INT_MSK0 | TX Queue#0 packet transmit interrupt<br>1 : Enable the interrupt<br>0 : Disable the interrupt             | 0x0 |
| 2 | RW | RX_DONE_INT_MSK  | RX packet receive interrupt<br>1 : Enable the interrupt<br>0 : Disable the interrupt                      | 0x0 |
| 1 | RW | TX_DLY_INT_MSK   | Summary of the whole WPDMA TX related interrupts<br>1 : Enable the interrupt<br>0 : Disable the interrupt | 0x0 |
| 0 | RW | RX_DLY_INT_MSK   | Summary of the whole WPDMA RX related interrupts<br>1 : Enable the interrupt<br>0 : Disable the interrupt | 0x0 |

**WPDMA\_GLO\_CFG: (offset: 0x0208)**

| Bits  | Type | Name          | Description                                                                                                                                                                                     | Initial value |
|-------|------|---------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:16 | -    | -             | Reserved                                                                                                                                                                                        | 0x0           |
| 15:8  | RW   | HDR_SEG_LEN   | Specify the header segment size in byte to support RX header/payload scattering function, when set to a non-zero value.<br>When set to zero, the header/payload scattering feature is disabled. | 0x0           |
| 7     | RW   | BIG_ENDIAN    | The endian mode selection. DMA applies the endian rule to convert payload and TX/RX information. DMA won't apply endian rule to register or descriptor. 1: big endian. 0: little endian.        | 0x0           |
| 6     | RW   | TX_WB_DDONE   | 0 :Disable TX_DMA writing back DDONE into TXD<br>1 : Enable TX_DMA writing back DDONE into TXD                                                                                                  | 0x1           |
| 5:4   | RW   | WPDMA_BT_SIZE | Define the burst size of WPDMA<br>0 : 4 DWORD (16bytes)<br>1 : 8 DWORD (32 bytes)<br>2 : 16 DWORD (64 bytes)<br>3 : 32 DWORD (128 bytes)                                                        | 0x2           |
| 3     | RO   | RX_DMA_BUSY   | 1 : RX_DMA is busy<br>0 : RX_DMA is not busy                                                                                                                                                    | 0x0           |
| 2     | RW   | RX_DMA_EN     | 1 : Enable RX_DMA<br>0 : Disable RX_DMA (when disabled, RX_DMA will finish the                                                                                                                  | 0x0           |

|   |    |             |                                                                                                                    |     |
|---|----|-------------|--------------------------------------------------------------------------------------------------------------------|-----|
|   |    |             | current receiving packet, then stop.)                                                                              |     |
| 1 | RO | TX_DMA_BUSY | 1 : TX_DMA is busy<br>0 : TX_DMA is not busy                                                                       | 0x0 |
| 0 | RW | TX_DMA_EN   | 1 : Enable TX_DMA<br>0 : Disable TX_DMA (when disabled, TX_DMA will finish the current sending packet, then stop.) | 0x0 |

**WPDMA\_RST\_IDX: (offset: 0x020c)**

| Bits  | Type | Name         | Description                            | Initial value |
|-------|------|--------------|----------------------------------------|---------------|
| 31:17 | -    | -            | Reserved                               | 0x0           |
| 16    | W1C  | RST_DRX_IDX0 | Write 1 to reset to RX_DMARX_IDX0 to 0 | 0x0           |
| 15:6  | -    | -            | Reserved                               | 0x0           |
| 5     | W1C  | RST_DTX_IDX3 | Write 1 to reset to TX_DMATX_IDX5 to 0 | 0x0           |
| 4     | W1C  | RST_DTX_IDX2 | Write 1 to reset to TX_DMATX_IDX4 to 0 | 0x0           |
| 3     | W1C  | RST_DTX_IDX3 | Write 1 to reset to TX_DMATX_IDX3 to 0 | 0x0           |
| 2     | W1C  | RST_DTX_IDX2 | Write 1 to reset to TX_DMATX_IDX2 to 0 | 0x0           |
| 1     | W1C  | RST_DTX_IDX1 | Write 1 to reset to TX_DMATX_IDX1 to 0 | 0x0           |
| 0     | W1C  | RST_DTX_IDX0 | Write 1 to reset to TX_DMATX_IDX0 to 0 | 0x0           |

**DELAY\_INT\_CFG: (offset: 0x0210)**

| Bits  | Type | Name         | Description                                                                                                                                                                                                                                                                                       | Initial value |
|-------|------|--------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31    | RW   | TXDLY_INT_EN | 1: Enable TX delayed interrupt mechanism.<br>0: Disable TX delayed interrupt mechanism.                                                                                                                                                                                                           | 0x0           |
| 30:24 | RW   | TXMAX_PINT   | Specified Max # of pended interrupts.<br>When the # of pended interrupts equal or grater than the value specified here or interrupt pending time reach the limit (See below), an Final TX_DLY_INT is generated.<br><br>Set to 0 will disable pending interrupt count check                        | 0x0           |
| 23:16 | RW   | TXMAX_PTIME  | Specified Max pending time for the internal TX_DONE_INT0-5.<br>When the pending time equal or grater TXMAX_PTIME x 20us or the # of pended TX_DONE_INT0-5 equal or grater than TXMAX_PINT (see above), an Final TX_DLY_INT is generated<br><br>Set to 0 will disable pending interrupt time check | 0x0           |
| 15    | RW   | RXDLY_INT_EN | 1: Enable RX delayed interrupt mechanism.<br>0: Disable RX delayed interrupt mechanism.                                                                                                                                                                                                           | 0x0           |
| 14:8  | RW   | RXMAX_PINT   | Specified Max # of pended interrupts.<br>When the # of pended interrupts equal or grater than the value specified here or interrupt pending time reach the limit (See below), an Final RX_DLY_INT is generated.<br><br>Set to 0 will disable pending interrupt count check                        | 0x0           |
| 7:0   | RW   | RXMAX_PTIME  | Specified Max pending time for the internal RX_DONE_INT. When the pending time equal or grater RXMAX_PTIME x 20us or , the # of pended RX_DONE_INT equal or grater than RXMAX_PCNT (see above), an Final RX_DLY_INT is generated<br><br>Set to 0 will disable pending interrupt time check        | 0x0           |

**WMM\_AIFSN\_CFG: (offset: 0x0214)**

| Bits  | Type | Name | Description | Initial value |
|-------|------|------|-------------|---------------|
| 31:16 | -    | -    | Reserved    | 0x0           |

|       |    |        |                      |     |
|-------|----|--------|----------------------|-----|
| 15:12 | RW | AIFSN3 | WMM parameter AIFSN3 | 0x0 |
| 11:8  | RW | AIFSN2 | WMM parameter AIFSN2 | 0x0 |
| 7:4   | RW | AIFSN1 | WMM parameter AIFSN1 | 0x0 |
| 3:0   | RW | AIFSN0 | WMM parameter AIFSN0 | 0x0 |

WMM\_CWMIN\_CFG: (offset: 0x0218)

| Bits  | Type | Name    | Description           | Initial value |
|-------|------|---------|-----------------------|---------------|
| 31:16 | -    | -       | Reserved              | 0x0           |
| 15:12 | RW   | CW_MIN3 | WMM parameter Cw_min3 | 0x0           |
| 11:8  | RW   | CW_MIN2 | WMM parameter Cw_min2 | 0x0           |
| 7:4   | RW   | CW_MIN1 | WMM parameter Cw_min1 | 0x0           |
| 3:0   | RW   | CW_MIN0 | WMM parameter Cw_min0 | 0x0           |

WMM\_CWMAX\_CFG: (offset: 0x021c)

| Bits  | Type | Name    | Description           | Initial value |
|-------|------|---------|-----------------------|---------------|
| 31:16 | -    | -       | Reserved              | 0x0           |
| 15:12 | RW   | CW_MAX3 | WMM parameter Cw_max3 | 0x0           |
| 11:8  | RW   | CW_MAX2 | WMM parameter Cw_max2 | 0x0           |
| 7:4   | RW   | CW_MAX1 | WMM parameter Cw_max1 | 0x0           |
| 3:0   | RW   | CW_MAX0 | WMM parameter Cw_max0 | 0x0           |

WMM\_TXOP0\_CFG: (offset: 0x0220)

| Bits  | Type | Name  | Description         | Initial value |
|-------|------|-------|---------------------|---------------|
| 31:16 | RW   | TXOP1 | WMM parameter TXOP1 | 0x0           |
| 15:0  | RW   | TXOP0 | WMM parameter TXOP0 | 0x0           |

WMM\_TXOP1\_CFG: (offset: 0x0224)

| Bits  | Type | Name  | Description         | Initial value |
|-------|------|-------|---------------------|---------------|
| 31:16 | RW   | TXOP3 | WMM parameter TXOP3 | 0x0           |
| 15:0  | RW   | TXOP2 | WMM parameter TXOP2 | 0x0           |

TX\_BASE\_PTRn: (offset: 0x0230, 0x0240, 0x0250, 0x0260, 0x0270, 0x0280)

| Bits | Type | Name         | Description                                                     | Initial value |
|------|------|--------------|-----------------------------------------------------------------|---------------|
| 31:0 | RW   | TX_BASE_PTRn | Point to the base address of TX_Ringn (4-DWORD aligned address) | 0x0           |

TX\_MAX\_CNTn: (offset: 0x0234, 0x0244, 0x0254, 0x0264, 0x0274, 0x0284)

| Bits  | Type | Name        | Description                                   | Initial value |
|-------|------|-------------|-----------------------------------------------|---------------|
| 31:12 | -    | -           | Reserved                                      | 0x0           |
| 11:0  | RW   | TX_MAX_CNTn | The maximum number of TXD count in TXD_Ringn. | 0x0           |

TX\_CTX\_IDXn: (offset: 0x0238, 0x0248, 0x0258, 0x0268, 0x0278, 0x0288)

| Bits  | Type | Name        | Description                            | Initial value |
|-------|------|-------------|----------------------------------------|---------------|
| 31:12 | -    | -           | Reserved                               | 0x0           |
| 11:0  | RW   | TX_CTX_IDXn | Point to the next TXD CPU wants to use | 0x0           |

TX\_DTX\_IDXn: (offset: 0x023c, 0x024c, 0x025c, 0x026c, 0x027c, 0x028c)

| Bits  | Type | Name        | Description                            | Initial value |
|-------|------|-------------|----------------------------------------|---------------|
| 31:12 | -    | -           | Reserved                               | 0x0           |
| 11:0  | RO   | TX_DTX_IDXn | Point to the next TXD DMA wants to use | 0x0           |

RX\_BASE\_PTR: (offset: 0x0290)

| Bits | Type | Name | Description | Initial value |
|------|------|------|-------------|---------------|
|------|------|------|-------------|---------------|

|      |    |              |                                                                                             |     |
|------|----|--------------|---------------------------------------------------------------------------------------------|-----|
| 31:0 | RW | RX_BASE_PTR0 | Point to the base address of RXD Ring #0 (GE ports). It should be a 4-DWORD aligned address | 0x0 |
|------|----|--------------|---------------------------------------------------------------------------------------------|-----|

RX\_MAX\_CNT: (offset: 0x0294)

| Bits  | Type | Name        | Description                                     | Initial value |
|-------|------|-------------|-------------------------------------------------|---------------|
| 31:12 | -    | -           | Reserved                                        | 0x0           |
| 11:0  | RW   | RX_MAX_CNT0 | The maximum number of RXD count in RXD Ring #0. | 0x0           |

RX\_CALC\_IDX: (offset: 0x0298)

| Bits  | Type | Name         | Description                                                 | Initial value |
|-------|------|--------------|-------------------------------------------------------------|---------------|
| 31:12 | -    | -            | Reserved                                                    | 0x0           |
| 11:0  | RW   | RX_CALC_IDX0 | Point to the next RXD CPU wants to allocate to RXD Ring #0. | 0x0           |

FS\_DRX\_IDX: (offset: 0x029c)

| Bits  | Type | Name        | Description                                                                                   | Initial value |
|-------|------|-------------|-----------------------------------------------------------------------------------------------|---------------|
| 31:12 | -    | -           | Reserved                                                                                      | 0x0           |
| 11:0  | RW   | RX_DRX_IDX0 | Point to the next RXD DMA wants to use in FDS Ring#0. It should be a 4-DWORD aligned address. | 0x0           |

US\_CYC\_CNT: (offset: 0x02a4)

| Bits  | Type | Name       | Description                                                                                                                                                  | Initial value |
|-------|------|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:25 | -    | -          | Reserved                                                                                                                                                     | 0x0           |
| 24    | RW   | TEST_EN    | Test mode enable                                                                                                                                             | 0x0           |
| 23:16 | RW   | TEST_SEL   | Test mode selection                                                                                                                                          | 0xf0          |
| 15:9  | -    | -          | Reserved                                                                                                                                                     | 0x0           |
| 8     | RW   | BT_MODE_EN | Blue-tooth mode enable                                                                                                                                       | 0x0           |
| 7:0   | RW   | US_CYC_CNT | Clock cycle count in 1us. It's dependent on the system clock rate.<br>For system clock rate = 125Mhz, set 8'h7D<br>For system clock rate = 133Mhz, set 8'h85 | 0x21          |

### 3.3.1.1 Register Description - PBF (base: 0x1018\_0000)

SYS\_CTRL: (offset: 0x0400)

| Bits  | Type | Name       | Description                                                                                                                                                                                                                                                                               | Initial value |
|-------|------|------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:20 | -    | -          | Reserved                                                                                                                                                                                                                                                                                  | 0x0           |
| 19    | RW   | SHR_MSEL   | Shared memory access selection.<br>0: address 0x4000 – 0x7FFF mapping to lower 16kB of shared memory<br>1: address 0x4000 – 0x7FFF mapping to higher 4kB of shared memory                                                                                                                 | 0x0           |
| 18:17 | RW   | PBF_MSEL   | Packet buffer memory access selection.<br>00: address 0x8000 – 0xFFFF mapping to 1 <sup>st</sup> 32kB of packet buffer.<br>01: address 0x8000 – 0xFFFF mapping to 2 <sup>nd</sup> 32kB of packet buffer.<br>10: address 0x8000 – 0xFFFF mapping to 3 <sup>rd</sup> 32kB of packet buffer. | 0x0           |
| 16    | RW   | HST_PM_SEL | Host program ram write selection.                                                                                                                                                                                                                                                         | 0x0           |
| 15    | -    | -          | Reserved                                                                                                                                                                                                                                                                                  | 0x0           |
| 14    | RW   | CAP_MODE   | Packet buffer capture mode.<br>0: packet buffer in normal mode.<br>1: packet buffer in BBP capture mode.                                                                                                                                                                                  | 0x0           |

|     |     |            |                                                                               |     |
|-----|-----|------------|-------------------------------------------------------------------------------|-----|
| 13  | -   | -          | Reserved                                                                      | 0x1 |
| 12  | RW  | CLKSELECT  | MAC/PBF clock source selection.<br>0: from PLL<br>1: from 40MHz clock input   | 0x0 |
| 11  | RW  | PBF_CLKEN  | PBF clock enable.                                                             | 0x0 |
| 10  | RW  | MAC_CLK_EN | MAC clock enable.                                                             | 0x0 |
| 9   | RW  | DMA_CLK_EN | DMA clock enable.                                                             | 0x0 |
| 8   | -   | -          | Reserved                                                                      | 0x0 |
| 7   | RW  | MCU_READY  | MCU ready. 8051 writes '1' to this bit to inform host internal MCU is ready.  | 0x0 |
| 6:5 | -   | -          | Reserved                                                                      | 0x0 |
| 4   | RW  | ASY_RESET  | ASYNC interface reset. Write '1' to this bit will put ASYNC into reset state. | 0x0 |
| 3   | RW  | PBF_RESET  | PBF hardware reset. Write '1' to this bit will put PBF into reset state.      | 0x0 |
| 2   | RW  | MAC_RESET  | MAC hardware reset. Write '1' to this bit will put MAC into reset state.      | 0x0 |
| 1   | RW  | DMA_RESET  | DMA hardware reset. Write '1' to this bit will put DMA into reset state.      | 0x0 |
| 0   | W1C | MCU_RESET  | MCU hardware reset. This bit will be auto-cleared after several clock cycles. | 0x0 |

**HOST\_CMD: (offset: 0x0404)**

| Bits | Type | Name    | Description                                                                 | Initial value |
|------|------|---------|-----------------------------------------------------------------------------|---------------|
| 31:0 | RW   | HST_CMD | Host command code. Host write this register will trigger interrupt to 8051. | 0x0           |

**PBF\_CFG: (offset: 0x0408)**

| Bits  | Type | Name         | Description                                                                                                                                                                                            | Initial value |
|-------|------|--------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:24 | -    | -            | Reserved                                                                                                                                                                                               | 0x0           |
| 23:21 | RW   | TX1Q_NUM     | Queue depth of Tx1Q. The maximum number is 7.                                                                                                                                                          | 0x7           |
| 20:16 | RW   | TX2Q_NUM     | Queue depth of Tx2Q. The maximum number is 20.                                                                                                                                                         | 0x14          |
| 15    | RW   | NULL0_MODE   | HCCA NULL0 frame auto mode. In this mode, NULL0 frame will be automatically transmitted if TXQ1 is enabled but empty. After NULL0 frame transmitted, TXQ1 will be disabled.<br>0: disable<br>1: enable | 0x0           |
| 14    | RW   | NULL1_MODE   | HCCA NULL1 frame auto mode. In this mode, all TXQ (0/1/2) will be disabled after NULL1 frame transmitted.<br>0: disable<br>1: enable                                                                   | 0x0           |
| 13    | RW   | RX_DROP_MODE | Rx drop mode. When set, PBF will drop Rx packet before into DMA.<br>0: normal mode<br>1: drop mode                                                                                                     | 0x0           |
| 12    | RW   | TX0Q_MODE    | Tx0Q operation mode.<br>0: auto mode<br>1: manual mode                                                                                                                                                 | 0x0           |
| 11    | RW   | TX1Q_MODE    | Tx1Q operation mode.<br>0: auto mode<br>1: manual mode                                                                                                                                                 | 0x0           |
| 10    | RW   | TX2Q_MODE    | Tx2Q operation mode.<br>0: auto mode                                                                                                                                                                   | 0x0           |



|     |    |           |                                                                                                      |     |
|-----|----|-----------|------------------------------------------------------------------------------------------------------|-----|
|     |    |           | 1: manual mode                                                                                       |     |
| 9   | RW | RX0Q_MODE | Rx0Q operation mode.<br>0: auto mode<br>1: manual mode                                               | 0x0 |
| 8   | RW | HCCA_MODE | HCCA auto mode. In this mode, TXQ1 will be enabled when CF-POLL arriving.<br>0: disable<br>1: enable | 0x0 |
| 7:5 | -  | -         | Reserved                                                                                             | 0x0 |
| 4   | RW | TX0Q_EN   | Tx0Q enable<br>0: disable<br>1: enable                                                               | 0x1 |
| 3   | RW | TX1Q_EN   | Tx1Q enable<br>0: disable<br>1: enable                                                               | 0x0 |
| 2   | RW | TX2Q_EN   | Tx2Q enable<br>0: disable<br>1: enable                                                               | 0x1 |
| 1   | RW | RX0Q_EN   | Rx0Q enable<br>0: disable<br>1: enable                                                               | 0x1 |
| 0   | -  | -         | Reserved                                                                                             | 0x0 |

MAX\_PCNT: (offset: 0x040c)

| Bits  | Type | Name          | Description                        | Initial value |
|-------|------|---------------|------------------------------------|---------------|
| 31:24 | RW   | MAX_TX0Q_PCNT | Maximum buffer page count of Tx0Q. | 0x1f          |
| 23:16 | RW   | MAX_TX1Q_PCNT | Maximum buffer page count of Tx1Q. | 0x3f          |
| 15:8  | RW   | MAX_TX2Q_PCNT | Maximum buffer page count of Tx2Q. | 0x9f          |
| 7:0   | RW   | MAX_RX0Q_PCNT | Maximum buffer page count of Rx0Q. | 0x9f          |

BUF\_CTRL: (offset: 0x0410)

| Bits  | Type | Name       | Description                                                                      | Initial value |
|-------|------|------------|----------------------------------------------------------------------------------|---------------|
| 31:12 | -    | -          | Reserved                                                                         | 0x0           |
| 11    | W1C  | WRITE_TX0Q | Manual write Tx0Q.                                                               | 0x0           |
| 10    | W1C  | WRITE_TX1Q | Manual write Tx1Q.                                                               | 0x0           |
| 9     | W1C  | WRITE_TX2Q | Manual write Tx2Q.                                                               | 0x0           |
| 8     | W1C  | WRITE_RX0Q | Manual write Rx0Q.                                                               | 0x0           |
| 7     | W1C  | NULL0_KICK | Kick out NULL0 frame. This bit will be cleared after NULL0 frame is transmitted. | 0x0           |
| 6     | W1C  | NULL1_KICK | Kick out NULL1 frame. This bit will be cleared after NULL1 frame is transmitted. | 0x0           |
| 5     | W1C  | BUF_RESET  | Buffer reset.                                                                    | 0x0           |
| 4     | -    | -          | Reserved                                                                         | 0x0           |
| 3     | W1C  | READ_TX0Q  | Manual read Tx0Q.                                                                | 0x0           |
| 2     | W1C  | READ_TX1Q  | Manual read Tx1Q.                                                                | 0x0           |
| 1     | W1C  | READ_TX2Q  | Manual read Tx2Q.                                                                | 0x0           |
| 0     | W1C  | READ_RX0Q  | Manual read Rx0Q.                                                                | 0x0           |

MCU\_INT\_STA: (offset: 0x0414)

| Bits  | Type | Name       | Description                | Initial value |
|-------|------|------------|----------------------------|---------------|
| 31:28 | -    | -          | Reserved                   | 0x0           |
| 27    | RW   | MAC_INT_11 | MAC interrupt 11: Reserved | 0x0           |
| 26    | RW   | MAC_INT_10 | MAC interrupt 10: Reserved | 0x0           |



|       |    |             |                                                   |     |
|-------|----|-------------|---------------------------------------------------|-----|
| 25    | RW | MAC_INT_9   | MAC interrupt 9: Reserved                         | 0x0 |
| 24    | RW | MAC_INT_8   | MAC interrupt 8: RX QoS CF-Poll interrupt         | 0x0 |
| 23    | RW | MAC_INT_7   | MAC interrupt 7: TXOP early termination interrupt | 0x0 |
| 22    | RW | MAC_INT_6   | MAC interrupt 6: TXOP early timeout interrupt     | 0x0 |
| 21    | RW | MAC_INT_5   | MAC interrupt 5: Reserved                         | 0x0 |
| 20    | RW | MAC_INT_4   | MAC interrupt 4: GP timer interrupt               | 0x0 |
| 19    | RW | MAC_INT_3   | MAC interrupt 3: Auto wakeup interrupt            | 0x0 |
| 18    | RW | MAC_INT_2   | MAC interrupt 2: TX status interrupt              | 0x0 |
| 17    | RW | MAC_INT_1   | MAC interrupt 1: Pre-TBTT interrupt               | 0x0 |
| 16    | RW | MAC_INT_0   | MAC interrupt 0: TBTT interrupt                   | 0x0 |
| 15    | RW | ADCL5H8_INT | RF ADC change from 5-bit to 8-bits interrupt      | 0x0 |
| 14    | RW | RX_SD_INT   | RF RX signal detection interrupt                  | 0x0 |
| 13:12 | -  | -           | Reserved                                          | 0x0 |
| 11    | RW | DTX0_INT    | DMA to TX0Q frame transfer complete interrupt.    | 0x0 |
| 10    | RW | DTX1_INT    | DMA to TX1Q frame transfer complete interrupt.    | 0x0 |
| 9     | RW | DTX2_INT    | DMA to TX2Q frame transfer complete interrupt.    | 0x0 |
| 8     | RW | DRX0_INT    | RX0Q to DMA frame transfer complete interrupt.    | 0x0 |
| 7     | RW | HCMD_INT    | Host command interrupt.                           | 0x0 |
| 6     | RW | NOTX_INT    | NULL0 frame Tx complete interrupt.                | 0x0 |
| 5     | RW | N1TX_INT    | NULL1 frame Tx complete interrupt.                | 0x0 |
| 4     | RW | BCNTX_INT   | Beacon frame Tx complete interrupt.               | 0x0 |
| 3     | RW | MTX0_INT    | TX0Q to MAC frame transfer complete interrupt.    | 0x0 |
| 2     | RW | MTX1_INT    | TX1Q to MAC frame transfer complete interrupt.    | 0x0 |
| 1     | RW | MTX2_INT    | TX2Q to MAC frame transfer complete interrupt.    | 0x0 |
| 0     | RW | MRX0_INT    | MAC to RX0Q frame transfer complete interrupt.    | 0x0 |

MCU\_INT\_ENA: (offset: 0x0418)

| Bits  | Type | Name         | Description                                           | Initial value |
|-------|------|--------------|-------------------------------------------------------|---------------|
| 31:28 | -    | -            | Reserved                                              | 0x0           |
| 27    | RW   | MAC_INT11_EN | MAC interrupt 11 enable                               | 0x0           |
| 26    | RW   | MAC_INT10_EN | MAC interrupt 10 enable                               | 0x0           |
| 25    | RW   | MAC_INT9_EN  | MAC interrupt 9 enable                                | 0x0           |
| 24    | RW   | MAC_INT8_EN  | MAC interrupt 8 enable                                | 0x0           |
| 23    | RW   | MAC_INT7_EN  | MAC interrupt 7 enable                                | 0x0           |
| 22    | RW   | MAC_INT6_EN  | MAC interrupt 6 enable                                | 0x0           |
| 21    | RW   | MAC_INT5_EN  | MAC interrupt 5 enable                                | 0x0           |
| 20    | RW   | MAC_INT4_EN  | MAC interrupt 4 enable                                | 0x0           |
| 19    | RW   | MAC_INT3_EN  | MAC interrupt 3 enable                                | 0x0           |
| 18    | RW   | MAC_INT2_EN  | MAC interrupt 2 enable                                | 0x0           |
| 17    | RW   | MAC_INT1_EN  | MAC interrupt 1 enable                                | 0x0           |
| 16    | RW   | MAC_INT0_EN  | MAC interrupt 0 enable                                | 0x0           |
| 15:12 | -    | -            | Reserved                                              | 0x0           |
| 11    | RW   | DTX0_INT_EN  | DMA to TX0Q frame transfer complete interrupt enable. | 0x0           |
| 10    | RW   | DTX1_INT_EN  | DMA to TX1Q frame transfer complete interrupt enable. | 0x0           |
| 9     | RW   | DTX2_INT_EN  | DMA to TX2Q frame transfer complete interrupt enable. | 0x0           |
| 8     | RW   | DRX0_INT_EN  | RX0Q to DMA frame transfer complete interrupt enable. | 0x0           |
| 7     | RW   | HCMD_INT_EN  | Host command interrupt enable.                        | 0x0           |
| 6     | RW   | NOTX_INT_EN  | NULL0 frame Tx complete interrupt enable.             | 0x0           |

|   |    |              |                                                       |     |
|---|----|--------------|-------------------------------------------------------|-----|
| 5 | RW | N1TX_INT_EN  | NULL1 frame Tx complete interrupt enable.             | 0x0 |
| 4 | RW | BCNTX_INT_EN | Beacon frame Tx complete interrupt enable.            | 0x0 |
| 3 | RW | MTX0_INT_EN  | TX0Q to MAC frame transfer complete interrupt enable. | 0x0 |
| 2 | RW | MTX1_INT_EN  | TX1Q to MAC frame transfer complete interrupt enable. | 0x0 |
| 1 | RW | MTX2_INT_EN  | TX2Q to MAC frame transfer complete interrupt enable. | 0x0 |
| 0 | RW | MRX0_INT_EN  | MAC to RX0Q frame transfer complete interrupt enable. | 0x0 |

TX0Q\_IO: (offset: 0x041c)

| Bits  | Type | Name    | Description                                         | Initial value |
|-------|------|---------|-----------------------------------------------------|---------------|
| 31:16 | -    | -       | Reserved                                            | 0x0           |
| 15:0  | RW   | TX0Q_IO | TX0Q IO port. This register is used in manual mode. | 0x0           |

TX1Q\_IO: (offset: 0x0420)

| Bits  | Type | Name    | Description                                         | Initial value |
|-------|------|---------|-----------------------------------------------------|---------------|
| 31:16 | -    | -       | Reserved                                            | 0x0           |
| 15:0  | RW   | TX1Q_IO | TX1Q IO port. This register is used in manual mode. | 0x0           |

TX2Q\_IO: (offset: 0x0424)

| Bits  | Type | Name    | Description                                         | Initial value |
|-------|------|---------|-----------------------------------------------------|---------------|
| 31:16 | -    | -       | Reserved                                            | 0x0           |
| 15:0  | RW   | TX2Q_IO | TX2Q IO port. This register is used in manual mode. | 0x0           |

RX0Q\_IO: (offset: 0x0428)

| Bits  | Type | Name    | Description                                         | Initial value |
|-------|------|---------|-----------------------------------------------------|---------------|
| 31:16 | -    | -       | Reserved                                            | 0x0           |
| 15:0  | RW   | RX0Q_IO | RX0Q IO port. This register is used in manual mode. | 0x0           |

BCN\_OFFSET0: (offset: 0x042c)

| Bits  | Type | Name        | Description                                                 | Initial value |
|-------|------|-------------|-------------------------------------------------------------|---------------|
| 31:24 | RW   | BCN3_OFFSET | Beacon #3 address offset in shared memory. Unit is 64 byte. | 0xec          |
| 23:16 | RW   | BCN2_OFFSET | Beacon #2 address offset in shared memory. Unit is 64 byte. | 0xe8          |
| 15:8  | RW   | BCN1_OFFSET | Beacon #1 address offset in shared memory. Unit is 64 byte. | 0xe4          |
| 7:0   | RW   | BCN0_OFFSET | Beacon #0 address offset in shared memory. Unit is 64 byte. | 0xe0          |

**Note1:** There are two beacon frame buffers on this chip. They are located at 0x4000 - 0x4FFF (SHR\_MSEL = 1) and 0x6000 - 0x7FFF (SHR\_MSEL = 0).

The physical address of beacon frame is calculated by:

If OFFSET < 0x40

Set SHR\_MSEL = 1 (SYS\_CTRL[19] = 1)

Beacon frame starting address = OFFSET \* 64 + 0x4000 (0x4000 - 0x4FFF)

Else if OFFSET >= 0x80

Set SHR\_MSEL = 0 (SYS\_CTRL[19] = 0)

Beacon frame starting address = OFFSET \* 64 + 0x4000 (0x6000 - 0x7FFF)

Else

This address can't be beacon buffer

BCN\_OFFSET1: (offset: 0x0430)

| Bits  | Type | Name        | Description                                                 | Initial value |
|-------|------|-------------|-------------------------------------------------------------|---------------|
| 31:24 | RW   | BCN7_OFFSET | Beacon #7 address offset in shared memory. Unit is 64 byte. | 0xfc          |
| 23:16 | RW   | BCN6_OFFSET | Beacon #6 address offset in shared memory. Unit is 64 byte. | 0xf8          |
| 15:8  | RW   | BCN5_OFFSET | Beacon #5 address offset in shared memory. Unit is 64 byte. | 0xf4          |
| 7:0   | RW   | BCN4_OFFSET | Beacon #4 address offset in shared memory. Unit is 64 byte. | 0xf0          |

TXRXQ\_STA: (offset: 0x0434)

| Bits  | Type | Name     | Description | Initial value |
|-------|------|----------|-------------|---------------|
| 31:24 | RO   | RX0Q_STA | RxQ status  | 0x22          |
| 23:16 | RO   | TX2Q_STA | Tx2Q status | 0x2           |
| 15:8  | RO   | TX1Q_STA | Tx1Q status | 0x2           |
| 7:0   | RO   | TX0Q_STA | Tx0Q status | 0x2           |

TXRXQ\_PCNT: (offset: 0x0438)

| Bits  | Type | Name      | Description        | Initial value |
|-------|------|-----------|--------------------|---------------|
| 31:24 | RO   | RX0Q_PCNT | Page count in RxQ  | 0x0           |
| 23:16 | RO   | TX2Q_PCNT | Page count in Tx2Q | 0x0           |
| 15:8  | RO   | TX1Q_PCNT | Page count in Tx1Q | 0x0           |
| 7:0   | RO   | TX0Q_PCNT | Page count in Tx0Q | 0x0           |

PBF\_DBG: (offset: 0x043c)

| Bits | Type | Name      | Description     | Initial value |
|------|------|-----------|-----------------|---------------|
| 31:8 | -    | -         | Reserved        | 0x0           |
| 7:0  | RO   | FREE_PCNT | Free page count | 0xfe          |

CAP\_CTRL: (offset: 0x0440)

| Bits  | Type | Name        | Description                                                                                                | Initial value |
|-------|------|-------------|------------------------------------------------------------------------------------------------------------|---------------|
| 31    | RW   | CAP_ADC_FEQ | Data source.<br>0: data from the ADC output<br>1: Data from the FEQ output                                 | 0x0           |
| 30    | WC   | CAP_START   | Data capture start<br>0: No action<br>1: Start data capture (cleared automatically after capture finished) | 0x0           |
| 29    | W1C  | MAN_TRIG    | Manual capture trigger                                                                                     | 0x0           |
| 28:16 | RW   | TRIG_OFFSET | Starting address offset before trigger point.                                                              | 0x140         |
| 15:13 | -    | -           | Reserved                                                                                                   | 0x0           |
| 12:0  | RO   | START_ADDR  | Starting address of captured data.                                                                         | 0x0           |

### 3.3.1.2 Register Description – RF TEST (base: 0x1018\_0000)

CSR\_RF\_CFG: (offset: 0x0500)

| Bits  | Type | Name                 | Description                                                                                                                                 | Initial value |
|-------|------|----------------------|---------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:18 | -    | -                    | Reserved                                                                                                                                    | 0x0           |
| 17    | RW   | RF_CSR_KICK          | Write – kick RF register read/write<br>0: do nothing 1: kick read/write process<br>Read – Polling RF register read/write<br>0: idle 1: busy | 0x0           |
| 16    | RW   | RF_CSR_WR            | 0: read 1: write                                                                                                                            | 0x0           |
| 15:14 | -    | -                    | Reserved                                                                                                                                    | 0x0           |
| 13:8  | RW   | TESTCSR_RFACC_REGNUM | RF register ID R0 ~ R63<br>0 for R0, 1 for R1 and so on.                                                                                    | 0x0           |
| 7:0   | RW   | RF_CSR_DATA          | Write – DATA written to RF<br>Read – DATA read from RF                                                                                      | 0x0           |

**3.3.1.3 Register Description - MAC (base: 0x1018\_0000)**

ASIC\_VER\_ID: (offset: 0x1000)

| Bits  | Type | Name   | Description       | Initial value |
|-------|------|--------|-------------------|---------------|
| 31:16 | RO   | VER_ID | ASIC version ID   | 0x2860        |
| 15:0  | RO   | REV_ID | ASIC reversion ID | 0x0101        |

MAC\_SYS\_CTRL: (offset: 0x1004)

| Bits | Type | Name         | Description                                                                                                                                                                         | Initial value |
|------|------|--------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:8 | -    | -            | Reserved                                                                                                                                                                            | 0x0           |
| 7    | RW   | RX_TS_EN     | Write 32-bit hardware RX timestamp instead of (RXWI->RSSI), and write (RXWI->RSSI) instead of (RXWI->SNR).<br><br>Note: For QA RX sniffer mode only.<br><br>1: enable<br>0: disable | 0x0           |
| 6    | RW   | WLAN_HALT_EN | Enable external WLAN halt control signal<br>1: enable<br>0: disable                                                                                                                 | 0x0           |
| 5    | RW   | PBF_LOOP_EN  | Packet buffer loop back enable (TX->RX)<br>1: enable<br>0: disable                                                                                                                  | 0x0           |
| 4    | RW   | CONT_TX_TEST | Continuous TX production test; override MAC_RX_EN, MAC_TX_EN<br>1: enable<br>0: disable                                                                                             | 0x0           |
| 3    | RW   | MAC_RX_EN    | MAC RX enable<br>1: enable<br>0: disable                                                                                                                                            | 0x0           |
| 2    | RW   | MAC_TX_EN    | MAC TX enable<br>1: enable<br>0: disable                                                                                                                                            | 0x0           |
| 1    | RW   | BBP_HRST     | BBP hard-reset<br>1: BBP in reset state<br>0: BBP in normal state<br><br>Note: Whole BBP including BBP registers will be reset.                                                     | 0x1           |
| 0    | RW   | MAC_SRST     | MAC soft-reset<br>1: MAC in reset state<br>0: MAC in normal state<br><br>Note: MAC registers and tables will <b>NOT</b> be reset.                                                   | 0x1           |

**Note:** MAC hard-reset is outside the scope of MAC registers.

MAC\_ADDR\_DW0: (offset: 0x1008)

| Bits  | Type | Name       | Description       | Initial value |
|-------|------|------------|-------------------|---------------|
| 31:24 | RW   | MAC_ADDR_3 | MAC address byte3 | 0x0           |
| 23:16 | RW   | MAC_ADDR_2 | MAC address byte2 | 0x0           |

|      |    |            |                   |     |
|------|----|------------|-------------------|-----|
| 15:8 | RW | MAC_ADDR_1 | MAC address byte1 | 0x0 |
| 7:0  | RW | MAC_ADDR_0 | MAC address byte0 | 0x0 |

MAC\_ADDR\_DW1: (offset: 0x100c)

| Bits  | Type | Name       | Description       | Initial value |
|-------|------|------------|-------------------|---------------|
| 31:16 | -    | -          | Reserved          | 0x0           |
| 15:8  | RW   | MAC_ADDR_5 | MAC address byte5 | 0x0           |
| 7:0   | RW   | MAC_ADDR_4 | MAC address byte4 | 0x0           |

**Note:** Byte0 is the first byte on network. Its LSB bit is the first bit on network. For a MAC address captured on the network with order 00:01:02:03:04:05, byte0=00, byte1=01 etc.

MAC\_BSSID\_DW0: (offset: 0x1010)

| Bits  | Type | Name    | Description | Initial value |
|-------|------|---------|-------------|---------------|
| 31:24 | RW   | BSSID_3 | BSSID byte3 | 0x0           |
| 23:16 | RW   | BSSID_2 | BSSID byte2 | 0x0           |
| 15:8  | RW   | BSSID_1 | BSSID byte1 | 0x0           |
| 7:0   | RW   | BSSID_0 | BSSID byte0 | 0x0           |

MAC\_BSSID\_DW1: (offset: 0x1014)

| Bits  | Type | Name             | Description                                                                                                                                                                                                                                                                                                                                                                                                           | Initial value |
|-------|------|------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:21 | -    | -                | Reserved                                                                                                                                                                                                                                                                                                                                                                                                              | 0x0           |
| 20:18 | RW   | MULTI_BCN_NUM    | Multiple BSSID Beacon number<br>0: one back-off beacon<br>1-7: SIFS-burst beacon count                                                                                                                                                                                                                                                                                                                                | 0x0           |
| 17:16 | RW   | MULTI_BSSID_MODE | Multiple BSSID mode<br><br>In multiple-BSSID AP mode, BSSID shall be the same as MAC_ADDR, that is, this device owns multiple MAC_ADDR in this mode.<br><br>The multiple MAC_ADDR/BSSID are distinguished by [bit2: bit0] of byte5.<br><br>0: 1-BSSID mode (BSS index = 0)<br>1: 2-BSSID mode (byte5.bit0 as BSS index)<br>2: 4-BSSID mode (byte5.bit1:0 as BSS index)<br>3: 8-BSSID mode (byte5.bit2:0 as BSS index) | 0x0           |
| 15:8  | RW   | BSSID_5          | BSSID byte5                                                                                                                                                                                                                                                                                                                                                                                                           | 0x0           |
| 7:0   | RW   | BSSID_4          | BSSID byte4                                                                                                                                                                                                                                                                                                                                                                                                           | 0x0           |

MAX\_LEN\_CFG: (offset: 0x1018)

| Bits  | Type | Name         | Description                                                                                                                         | Initial value |
|-------|------|--------------|-------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:20 | -    | -            | Reserved                                                                                                                            | 0x0           |
| 19:16 | RW   | MIN_MPDU_LEN | Minimum MPDU length (unit: bytes)<br><br>MAC will drop the MPDU if the length is less than this limitation. Applied only in MAC RX. | 0xa           |
| 15:14 | -    | -            | Reserved                                                                                                                            | 0x0           |

|       |    |              |                                                                                                                                                                                                                                                                                     |        |
|-------|----|--------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|
| 13:12 | RW | MAX_PSDU_LEN | Maximum PSDU length (power factor)<br><br>0: 2 <sup>13</sup> = 8K bytes<br>1: 2 <sup>14</sup> = 16K bytes<br>2: 2 <sup>15</sup> = 32K bytes<br>3: 2 <sup>16</sup> = 64K bytes<br><br>MAC will NOT generate A-MPDU with length greater than this limitation. Applied only in MAC TX. | 0x0    |
| 11:0  | RW | MAX_MPDU_LEN | Maximum MPDU length (unit: bytes)<br><br>MAC will drop the MPDU if the length is greater than this limitation. Applied only in MAC RX.                                                                                                                                              | 0xffff |

BBP\_CSR\_CFG: (offset: 0x101c)

| Bits  | Type | Name         | Description                                                                                                                                                 | Initial value |
|-------|------|--------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:20 | -    | -            | Reserved                                                                                                                                                    | 0x0           |
| 19    | RW   | BBP_RW_MODE  | BBP Register R/W mode<br>1: parallel mode<br>0: serial mode                                                                                                 | 0x1           |
| 18    | RW   | BBP_PAR_DUR  | BBP Register parallel R/W pulse width<br>0: pulse width = 62.5ns<br>1: pulse width = 112.5ns<br><br><b>Note:</b> Please set BBP_PAR_DUR=1 in 802.11J mode.  | 0x0           |
| 17    | RW   | BBP_CSR_KICK | Write - kick BBP register read/write<br>0: do nothing 1: kick read/write process<br><br>Read - Polling BBP register read/write progress<br>0: idle, 1: busy | 0x0           |
| 16    | RW   | BBP_CSR_RW   | 0: Write<br>1: Read                                                                                                                                         | 0x0           |
| 15:8  | RW   | BBP_ADDR     | BBP register ID<br>0 for R0, 1 for R1, and so on.                                                                                                           | 0x0           |
| 7:0   | RW   | BBP_DATA     | Write - Data written to BBP<br>Read - Data read from BBP                                                                                                    | 0x0           |

RF\_CSR\_CFG0: (offset: 0x1020)

| Bits  | Type | Name         | Description                                                                         | Initial value |
|-------|------|--------------|-------------------------------------------------------------------------------------|---------------|
| 31    | RW   | RF_REG_CTRL  | Write: 1 - RF_REG0/1/2 to RF chip<br>Read: 0 - idle, 1 - busy                       | 0x0           |
| 30    | RW   | RF_LE_SEL    | RF_LE selection<br>0: RF_LE0 activate<br>1: RF_LE1 activate                         | 0x0           |
| 29    | RW   | RF_LE_STBY   | RF_LE standby mode<br>0: RF_LE is high when standby<br>1: RF_LE is low when standby | 0x0           |
| 28:24 | RW   | RF_REG_WIDTH | RF register bit width<br>Default: 22                                                | 0x16          |
| 23:0  | RW   | RF_REG_0     | RF register0 ID and content                                                         | 0x0           |

**RF\_CSR\_CFG1: (offset: 0x1024)**

| Bits  | Type | Name     | Description                                                                                                     | Initial value |
|-------|------|----------|-----------------------------------------------------------------------------------------------------------------|---------------|
| 31:25 | -    | -        | Reserved                                                                                                        | 0x0           |
| 24    | RW   | RF_DUR   | Gap between BB_CONTROL_RF and RF_LE<br>0: 3 system clock cycle (37.5usec)<br>1: 5 system clock cycle (62.5usec) | 0x0           |
| 23:0  | RW   | RF_REG_1 | RF register1 ID and content                                                                                     | 0x0           |

**RF\_CSR\_CFG2: (offset: 0x1028)**

| Bits  | Type | Name     | Description                 | Initial value |
|-------|------|----------|-----------------------------|---------------|
| 31:24 | -    | -        | Reserved                    | 0x0           |
| 23:0  | RW   | RF_REG_2 | RF register2 ID and content | 0x0           |

**Note:** Software should make sure the first bit (MSB in the specified bit number) written to RF is 0 for RF chip mode selection.

**LED\_CFG: (offset: 0x102c)**

| Bits  | Type | Name          | Description                                                                                   | Initial value |
|-------|------|---------------|-----------------------------------------------------------------------------------------------|---------------|
| 31    | -    | -             | Reserved                                                                                      | 0x0           |
| 30    | RW   | LED_POL       | LED polarity<br>0: active low<br>1: active high                                               | 0x0           |
| 29:28 | RW   | Y_LED_MODE    | Yellow LED mode<br>0: off<br>1: blinking upon TX<br>2: periodic slow blinking<br>3: always on | 0x0           |
| 27:26 | RW   | G_LED_MODE    | Green LED mode<br>0: off<br>1: blinking upon TX<br>2: periodic slow blinking<br>3: always on  | 0x2           |
| 25:24 | RW   | R_LED_MODE    | Red LED mode<br>0: off<br>1: blinking upon TX<br>2: periodic slow blinking<br>3: always on    | 0x1           |
| 23:22 | -    | -             | Reserved                                                                                      | 0x0           |
| 21:16 | RW   | SLOW_BLK_TIME | Slow blinking period (unit: 1sec)                                                             | 0x3           |
| 15:8  | RW   | LED_OFF_TIME  | TX blinking off period (unit: 1ms)                                                            | 0x1e          |
| 7:0   | RW   | LED_ON_TIME   | TX blinking on period (unit: 1ms)                                                             | 0x46          |

**XIFS\_TIME\_CFG: (offset: 0x1100)**

| Bits  | Type | Name        | Description             | Initial value |
|-------|------|-------------|-------------------------|---------------|
| 31:30 | -    | -           | Reserved                | 0x0           |
| 29    | RW   | BB_RXEND_EN | BB_RX_END signal enable | 0x11          |



|       |    |                |                                                                                                                                                                |       |
|-------|----|----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|
|       |    |                | Refer BB_RX_END signal from BBP RX logic to start SIFS defer.<br><br>0: disable<br>1: enable                                                                   |       |
| 28:20 | RW | EIFS_TIME      | EIFS time (unit: 1us)<br><br>EIFS is the defer time after reception of a CRC error packet.<br>After deferring EIFS, the normal back-off process may proceed.   | 0x13a |
| 19:16 | RW | OFDM_XIFS_TIME | Delayed OFDM SIFS time compensator (unit: 1us)<br><br>When BB_RX_END from BBP is a delayed version the SIFS deferred will be (OFDM_SIFS_TIME - OFDM_XIFS_TIME) | 0x4   |
| 15:8  | RW | OFDM_SIFS_TIME | OFDM SIFS time (unit: 1us)<br><br>Applied after OFDM TX/RX.                                                                                                    | 0x10  |
| 7:0   | RW | CCK_SIFS_TIME  | CCK SIFS time (unit: 1us)<br><br>Applied after CCK TX/RX.                                                                                                      | 0xa   |

**Note1:** EIFS = SIFS + ACK @ 1Mbps + DIFS = 10us (SIFS) + 192us (long preamble) + 14\*8us (ACK) + 50us (DIFS) = 364. However, MAC should start back-off procedure after (EIFS-DIFS).

**Note2:** EIFS is not applied if MAC is a TXOP initiator that owns the channel.

**Note3:** EIFS is not started if AMPDU is only partial corrupted.

**Caution:** It is recommended that both (CCK\_SIFS\_TIME) and (OFDM\_SIFS\_TIME) are no less than TX/RX transition time. If the SIFS value is not long enough, a SIFS burst transmission may be replaced with a PIFS burst one.

BKOFF\_SLOT\_CFG: (offset:0x1104)

| Bits  | Type | Name          | Description                                                                                                                                                                        | Initial value |
|-------|------|---------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:12 | -    | -             | Reserved                                                                                                                                                                           | 0x0           |
| 11:8  | RW   | CC_DELAY_TIME | Channel clear delay (unit: 1-us)<br><br>This value specified the TX guard time after channel is clear.                                                                             | 0x2           |
| 7:0   | RW   | SLOT_TIME     | Slot time (unit: 1-us)<br><br>This value specified the slot boundary after deferring SIFS time.<br><br><b>Note:</b> Default 20us is for 11b/g. 11a and 11g-short-slot-mode is 9us. | 0x14          |

NAV\_TIME\_CFG: (offset: 0x1108)

| Bits  | Type | Name        | Description                                                                                                                                                        | Initial value |
|-------|------|-------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31    | WC   | NAV_UPD     | NAV timer manual update command<br><br>0: Do nothing<br>1: Update NAV timer with NAV_UPD_VAL                                                                       | 0x0           |
| 30:16 | RW   | NAV_UPD_VAL | NAV timer manual update value (unit: 1us)                                                                                                                          | 0x0           |
| 15    | RW   | NAV_CLR_EN  | NAV timer auto-clear enable<br><br>When enabled, MAC will auto clear NAV timer after the reception of CF-End frame from previous NAV holder STA.<br><br>0: disable | 0x1           |



|      |    |           |                                                                                                                                                                                                              |     |
|------|----|-----------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|
|      |    |           | 1: enable                                                                                                                                                                                                    |     |
| 14:0 | RO | NAV_TIMER | NAV timer (unit: 1us)<br><br>The timer is set by other STA and will auto countdown to zero. The STA who set the NAV timer is called the NAV holder. When NAV timer is nonzero, MAC will not send any packet. | 0x0 |

**CH\_TIME\_CFG: (offset: 0x110c)**

| Bits | Type | Name            | Description                                               | Initial value |
|------|------|-----------------|-----------------------------------------------------------|---------------|
| 31:5 | -    | -               | Reserved                                                  | 0x0           |
| 4    | RW   | EIFS_AS_CH_BUSY | Count EIFS as channel busy<br>0: disable<br>1: enable     | 0x1           |
| 3    | RW   | NAV_AS_CH_BUSY  | Count NAV as channel busy<br>0: disable<br>1: enable      | 0x1           |
| 2    | RW   | RX_AS_CH_BUSY   | Count RX busy as channel busy<br>0: disable<br>1: enable  | 0x1           |
| 1    | RW   | TX_AS_CH_BUSY   | Count TX busy as channel busy<br>0: disable<br>1: enable  | 0x1           |
| 0    | RW   | CH_STA_TIMER_EN | Channel statistic timer enable<br>0: disable<br>1: enable | 0x0           |

**PBF\_LIFE\_TIMER: (offset: 0x1110)**

| Bits | Type | Name           | Description                                        | Initial value |
|------|------|----------------|----------------------------------------------------|---------------|
| 31:0 | RO   | PBF_LIFE_TIMER | TX/RX MPDU timestamp timer (free run)<br>Unit: 1us | 0x0           |

**BCN\_TIME\_CFG: (offset: 0x1114)**

| Bits  | Type | Name          | Description                                                                                                                            | Initial value |
|-------|------|---------------|----------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:24 | RW   | TSF_INS_COMP  | TSF insertion compensation value (unit: 1us)<br><br>When inserting TSF, add this value with local TSF timer as the TX timestamp.       | 0x0           |
| 23:21 | -    | -             | Reserved                                                                                                                               | 0x0           |
| 20    | RW   | BCN_TX_EN     | BEACON frame TX enable<br><br>When enabled, MAC sends BEACON frame at TBTT interrupt.<br>0: disable<br>1: enable                       | 0x0           |
| 19    | RW   | TBTT_TIMER_EN | TBTT timer enable<br><br>When enabled, TBTT interrupt will be issued periodically with period specified in (BCN_INTVAL).<br>0: disable | 0x0           |

|       |    |               |                                                                                                                                                                                                                                                                                                                                                                                                                 |       |
|-------|----|---------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|
|       |    |               | 1: enable                                                                                                                                                                                                                                                                                                                                                                                                       |       |
| 18:17 | RW | TSF_SYNC_MODE | Local 64-bit TSF timer synchronization mode<br><br>00: disable<br>01: (STA infra-structure mode) Upon the reception of BEACON frame from associated BSS, local TSF is always updated with remote TSF.<br>10: (STA ad-hoc mode) Upon the reception of BEACON frame from associated BSS, local TSF is updated with remote TSF only if the remote TSF is greater than local TSF.<br>11: (AP mode) SYNC with nobody | 0x0   |
| 16    | RW | TSF_TIMER_EN  | Local 64-bit TSF timer enable<br><br>When enabled, TSF timer will re-start from zero.<br><br>0: disable<br>1: enable                                                                                                                                                                                                                                                                                            | 0x0   |
| 15:0  | RW | BCN_INTVAL    | BEACON interval (unit: 64us)<br><br>This value specified the interval between<br><br>Maximum beacon interval is about 4sec.                                                                                                                                                                                                                                                                                     | 0x640 |

**TBTT\_SYNC\_CFG: (offset: 0x1118)**

| Bits  | Type | Name        | Description                                                                                                                                                                                                                                                 | Initial value |
|-------|------|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:24 | -    | -           | Reserved                                                                                                                                                                                                                                                    | 0x0           |
| 23:20 | RW   | BCN_CWMIN   | Beacon transmission CWMIN after TBTT interrupt (unit: slot)                                                                                                                                                                                                 | 0x4           |
| 19:16 | RW   | BCN_AIFSN   | Beacon transmission AIFSN after TBTT interrupt (unit: slot)                                                                                                                                                                                                 | 0x2           |
| 15:8  | RW   | BCN_EXP_WIN | Beacon expecting window duration (unit: 64us)<br><br>The window starts from TBTT interrupt. The phase of "TBTT interrupt train" will NOT be adjusted by the beacon arrived within the window.                                                               | 0x20          |
| 7:0   | RW   | TBTT_ADJUST | IBSS mode TBTT phase adaptive adjustment step (unit: 1us), default value is 16us.<br><br>In IBSS mode (Ad hoc), if consecutive TX beacon failures (or consecutive success) happened, TBTT timer will adjust it phase to meet the external Ad hoc TBTT time. | 0x10          |

**TSF\_TIMER\_DW0: (offset: 0x111c)**

| Bits | Type | Name          | Description                             | Initial value |
|------|------|---------------|-----------------------------------------|---------------|
| 31:0 | RO   | TSF_TIMER_DW0 | Local TSF timer LSB 32 bits (unit: 1us) | 0x0           |

**TSF\_TIMER\_DW1: (offset: 0x1120)**

| Bits | Type | Name          | Description                             | Initial value |
|------|------|---------------|-----------------------------------------|---------------|
| 31:0 | RO   | TSF_TIMER_DW1 | Local TSF timer MSB 32 bits (unit: 1us) | 0x0           |

**TBTT\_TIMER: (offset: 0x1124)**

| Bits  | Type | Name | Description | Initial value |
|-------|------|------|-------------|---------------|
| 31:17 | -    | -    | Reserved    | 0x0           |

|      |    |            |                                                                                                                                                                                                                                     |     |
|------|----|------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|
| 16:0 | RO | TBTT_TIMER | <p>TBTT Timer (unit: 32us)</p> <p>The time remains till next TBTT.</p> <p>When TBTT_TIMER_EN is enabled, the timer will down count from BCN_INTVAL to zero.</p> <p>When TBTT_TIMER_EN is disabled, the timer will stay in zero.</p> | 0x0 |
|------|----|------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|

**INT\_TIMER\_CFG: (offset: 0x1128)**

| Bits  | Type | Name           | Description                                                                                                        | Initial value |
|-------|------|----------------|--------------------------------------------------------------------------------------------------------------------|---------------|
| 31:16 | RW   | GP_TIMER       | <p>Period of general purpose interrupt timer</p> <p>(Unit: 64us)</p>                                               | 0x0           |
| 15:0  | RW   | PRE_TBTT_TIMER | <p>Pre-TBTT interrupt time (unit: 64us)</p> <p>The value specified the interrupt timing before TBTT interrupt.</p> | 0x0           |

**INT\_TIMER\_EN: (offset: 0x112c)**

| Bits | Type | Name            | Description                                                                            | Initial value |
|------|------|-----------------|----------------------------------------------------------------------------------------|---------------|
| 31:2 | -    | -               | Reserved                                                                               | 0x0           |
| 1    | RW   | GP_TIMER_EN     | <p>Periodic general purpose interrupt timer enable</p> <p>0: disable<br/>1: enable</p> | 0x0           |
| 0    | RW   | PRE_TBTT_INT_EN | <p>Pre-TBTT interrupt enable</p> <p>0: disable<br/>1: enable</p>                       | 0x0           |

**CH\_IDLE\_STA: (offset: 0x1130)**

| Bits | Type | Name         | Description                               | Initial value |
|------|------|--------------|-------------------------------------------|---------------|
| 31:0 | RC   | CH_IDLE_TIME | <p>Channel idle time</p> <p>Unit: 1us</p> | 0x0           |

In application, the channel busy time can be derived by the equation:

$$CH\_BUSY\_TIME = \text{host polling period} - CH\_IDLE\_TIME$$

**Reserved: (offset: 0x1134)**

| Bits | Type | Name | Description | Initial value |
|------|------|------|-------------|---------------|
| 31:0 | -    | -    | Reserved    | 0x0           |

**MAC\_STATUS\_REG: (offset: 0x1200)**

| Bits | Type | Name      | Description                                 | Initial value |
|------|------|-----------|---------------------------------------------|---------------|
| 31:2 | -    | -         | Reserved                                    | 0x0           |
| 1    | RO   | RX_STATUS | <p>RX status</p> <p>0: Idle<br/>1: Busy</p> | 0x0           |
| 0    | RO   | TX_STATUS | TX status                                   | 0x0           |

|  |  |  |                    |  |
|--|--|--|--------------------|--|
|  |  |  | 0: Idle<br>1: Busy |  |
|--|--|--|--------------------|--|

**PWR\_PIN\_CFG: (offset: 0x1204)**

| Bits | Type | Name       | Description      | Initial value |
|------|------|------------|------------------|---------------|
| 31:4 | -    | -          | Reserved         | 0x0           |
| 3    | RW   | IO_ADDA_PD | AD/DA power down | 0x0           |
| 2    | RW   | IO_PLL_PD  | PLL power down   | 0x0           |
| 1    | RW   | IO_RA_PE   | RA_PE            | 0x1           |
| 0    | RW   | IO_RF_PE   | RF_PE            | 0x1           |

**AUTO\_WAKEUP\_CFG: (offset: 0x1208)**

| Bits  | Type | Name             | Description                                                                                                                                                                                                                                              | Initial value |
|-------|------|------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:16 | -    | -                | Reserved                                                                                                                                                                                                                                                 | 0x0           |
| 15    | RW   | AUTO_WAKEUP_EN   | Auto wakeup interrupt enable<br><br>Auto wakeup interrupt will be issued after #(SLEEP_TBTT_NUM) TBTTs' at WAKEUP_LEAD_TIME before the target wakeup TBTT.<br><br>0: disable<br>1: enable<br><br><b>Note:</b> Please make sure TBTT_TIMER_EN is enabled. | 0x0           |
| 14:8  | RW   | SLEEP_TBTT_NUM   | Number of sleeping TBTT                                                                                                                                                                                                                                  | 0x0           |
| 7:0   | RW   | WAKEUP_LEAD_TIME | Auto wakeup lead time (unit: 1TU=1024us)                                                                                                                                                                                                                 | 0x14          |

**5.17.5.3 MAC TX configuration registers (offset: 0x1300)**
**EDCA\_ACO\_CFG (BE): (offset: 0x1300)**

| Bits  | Type | Name      | Description                      | Initial value |
|-------|------|-----------|----------------------------------|---------------|
| 31:20 | -    | -         | Reserved                         | 0x0           |
| 19:16 | RW   | ACO_CWMAX | ACO CWMAX (unit: power of 2)     | 0x7           |
| 15:12 | RW   | ACO_CWMIN | ACO CWMIN (unit: power of 2)     | 0x3           |
| 11:8  | RW   | ACO_AIFSN | ACO AIFSN (unit: # of slot time) | 0x2           |
| 7:0   | RW   | ACO_TXOP  | ACO TXOP limit (unit: 32us)      | 0x0           |

**EDCA\_AC1\_CFG (BK): (offset: 0x1304)**

| Bits  | Type | Name      | Description                      | Initial value |
|-------|------|-----------|----------------------------------|---------------|
| 31:20 | -    | -         | Reserved                         | 0x0           |
| 19:16 | RW   | AC1_CWMAX | AC1 CWMAX (unit: power of 2)     | 0x7           |
| 15:12 | RW   | AC1_CWMIN | AC1 CWMIN (unit: power of 2)     | 0x3           |
| 11:8  | RW   | AC1_AIFSN | AC1 AIFSN (unit: # of slot time) | 0x2           |
| 7:0   | RW   | AC1_TXOP  | AC1 TXOP limit (unit: 32us)      | 0x0           |

**EDCA\_AC2\_CFG (VI): (offset: 0x1308)**

| Bits  | Type | Name      | Description                  | Initial value |
|-------|------|-----------|------------------------------|---------------|
| 31:20 | -    | -         | Reserved                     | 0x0           |
| 19:16 | RW   | AC2_CWMAX | AC2 CWMAX (unit: power of 2) | 0x7           |

|       |    |           |                                  |     |
|-------|----|-----------|----------------------------------|-----|
| 15:12 | RW | AC2_CWMIN | AC2 CWMIN (unit: power of 2)     | 0x3 |
| 11:8  | RW | AC2_AIFSN | AC2 AIFSN (unit: # of slot time) | 0x2 |
| 7:0   | RW | AC2_TXOP  | AC2 TXOP limit (unit: 32us)      | 0x0 |

EDCA\_AC3\_CFG (VO): (offset: 0x130c)

| Bits  | Type | Name      | Description                      | Initial value |
|-------|------|-----------|----------------------------------|---------------|
| 31:20 | -    | -         | Reserved                         | 0x0           |
| 19:16 | RW   | AC3_CWMAX | AC3 CWMAX (unit: power of 2)     | 0x7           |
| 15:12 | RW   | AC3_CWMIN | AC3 CWMIN (unit: power of 2)     | 0x3           |
| 11:8  | RW   | AC3_AIFSN | AC3 AIFSN (unit: # of slot time) | 0x2           |
| 7:0   | RW   | AC3_TXOP  | AC3 TXOP limit (unit: 32us)      | 0x0           |

EDCA\_TID\_AC\_MAP: (offset: 0x1310)

| Bits  | Type | Name        | Description       | Initial value |
|-------|------|-------------|-------------------|---------------|
| 31:16 | -    | -           | Reserved          | 0x0           |
| 15:14 | RW   | TID7_AC_MAP | AC value as TID=7 | 0x3           |
| 13:12 | RW   | TID6_AC_MAP | AC value as TID=6 | 0x3           |
| 11:10 | RW   | TID5_AC_MAP | AC value as TID=5 | 0x2           |
| 9:8   | RW   | TID4_AC_MAP | AC value as TID=4 | 0x2           |
| 7:6   | RW   | TID3_AC_MAP | AC value as TID=3 | 0x0           |
| 5:4   | RW   | TID2_AC_MAP | AC value as TID=2 | 0x1           |
| 3:2   | RW   | TID1_AC_MAP | AC value as TID=1 | 0x1           |
| 1:0   | RW   | TID0_AC_MAP | AC value as TID=0 | 0x0           |

Note: default according 802.11e Table 20.23—User priority to Access Category mappings

TX\_PWR\_CFG\_0: (offset: 0x1314)

| Bits  | Type | Name           | Description               | Initial value |
|-------|------|----------------|---------------------------|---------------|
| 31:24 | RW   | TX_PWR_OFDM_12 | TX power for OFDM 12M/18M | 0x66          |
| 23:16 | RW   | TX_PWR_OFDM_6  | TX power for OFDM 6M/9M   | 0x66          |
| 15:8  | RW   | TX_PWR_CCK_5   | TX power for CCK5.5M/11M  | 0x66          |
| 7:0   | RW   | TX_PWR_CCK_1   | TX power for CCK1M/2M     | 0x66          |

TX\_PWR\_CFG\_1: (offset: 0x1318)

| Bits  | Type | Name           | Description               | Initial value |
|-------|------|----------------|---------------------------|---------------|
| 31:24 | RW   | TX_PWR_MCS_2   | TX power for HT MCS=2,3   | 0x66          |
| 23:16 | RW   | TX_PWR_MCS_0   | TX power for HT MCS=0,1   | 0x66          |
| 15:8  | RW   | TX_PWR_OFDM_48 | TX power for OFDM 48M/54M | 0x66          |
| 7:0   | RW   | TX_PWR_OFDM_24 | TX power for OFDM 24M/36M | 0x66          |

TX\_PWR\_CFG\_2: (offset: 0x131c)

| Bits  | Type | Name          | Description               | Initial value |
|-------|------|---------------|---------------------------|---------------|
| 31:24 | RW   | TX_PWR_MCS_10 | TX power for HT MCS=10,11 | 0x66          |
| 23:16 | RW   | TX_PWR_MCS_8  | TX power for HT MCS=8,9   | 0x66          |
| 15:8  | RW   | TX_PWR_MCS_6  | TX power for HT MCS=6,7   | 0x66          |
| 7:0   | RW   | TX_PWR_MCS_4  | TX power for HT MCS=4,5   | 0x66          |

TX\_PWR\_CFG\_3: (offset: 0x1320)

| Bits  | Type | Name          | Description               | Initial value |
|-------|------|---------------|---------------------------|---------------|
| 31:24 | -    | -             | Reserved                  | 0x66          |
| 23:16 | -    | -             | Reserved                  | 0x66          |
| 15:8  | RW   | TX_PWR_MCS_14 | TX power for HT MCS=14,15 | 0x66          |
| 7:0   | RW   | TX_PWR_MCS_12 | TX power for HT MCS=12,13 | 0x66          |

TX\_PWR\_CFG\_4: (offset: 0x1324)

| Bits  | Type | Name | Description | Initial value |
|-------|------|------|-------------|---------------|
| 31:16 | -    | -    | Reserved    | 0x0           |
| 15:8  | -    | -    | Reserved    | 0x66          |
| 7:0   | -    | -    | Reserved    | 0x66          |

TX\_PIN\_CFG: (offset: 0x1328)

| Bits  | Type | Name          | Description        | Initial value |
|-------|------|---------------|--------------------|---------------|
| 31:20 | -    | -             | Reserved           | 0x0           |
| 19    | RW   | TRSW_POL      | TRSW_EN polarity   | 0x0           |
| 18    | RW   | TRSW_EN       | TRSW_EN enable     | 0x1           |
| 17    | RW   | RFTR_POL      | RF_TR polarity     | 0x0           |
| 16    | RW   | RFTR_EN       | RF_TR enable       | 0x1           |
| 15    | RW   | LNA_PE_G1_POL | LNA_PE_G1 polarity | 0x0           |
| 14    | RW   | LNA_PE_A1_POL | LNA_PE_A1 polarity | 0x0           |
| 13    | RW   | LNA_PE_G0_POL | LNA_PE_G0 polarity | 0x0           |
| 12    | RW   | LNA_PE_A0_POL | LNA_PE_A0 polarity | 0x0           |
| 11    | RW   | LNA_PE_G1_EN  | LNA_PE_G1 enable   | 0x1           |
| 10    | RW   | LNA_PE_A1_EN  | LNA_PE_A1 enable   | 0x1           |
| 9     | RW   | LNA_PE_G0_EN  | LNA_PE_G0 enable   | 0x1           |
| 8     | RW   | LNA_PE_A0_EN  | LNA_PE_A0 enable   | 0x1           |
| 7     | RW   | PA_PE_G1_POL  | PA_PE_G1 polarity  | 0x0           |
| 6     | RW   | PA_PE_A1_POL  | PA_PE_A1 polarity  | 0x0           |
| 5     | RW   | PA_PE_G0_POL  | PA_PE_G0 polarity  | 0x0           |
| 4     | RW   | PA_PE_A0_POL  | PA_PE_A0 polarity  | 0x0           |
| 3     | RW   | PA_PE_G1_EN   | PA_PE_G1 enable    | 0x1           |
| 2     | RW   | PA_PE_A1_EN   | PA_PE_A1 enable    | 0x1           |
| 1     | RW   | PA_PE_G0_EN   | PA_PE_G0 enable    | 0x1           |
| 0     | RW   | PA_PE_A0_EN   | PA_PE_A0 enable    | 0x1           |

TX\_BAND\_CFG: (offset: 0x132c)

| Bits | Type | Name          | Description                                                                | Initial value |
|------|------|---------------|----------------------------------------------------------------------------|---------------|
| 31:3 | -    | -             | Reserved                                                                   | 0x0           |
| 2    | RW   | 5G_BAND_SEL_N | 5G band selection PIN (complement of 5G_BAND_SEL_P)                        | 0x1           |
| 1    | RW   | 5G_BAND_SEL_P | 5G band selection PIN                                                      | 0x0           |
| 0    | RW   | TX_BAND_SEL   | 0: use lower 40Mhz band in 20Mhz TX<br>1: use upper 40Mhz band in 20Mhz TX | 0x0           |

Note1: TX\_BAND\_SEL is effective only when TX/RX bandwidth control register R4 of BBP is set to 40Mhz.

TX\_SW\_CFG0: (offset: 0x1330)

| Bits  | Type | Name        | Description              | Initial value |
|-------|------|-------------|--------------------------|---------------|
| 31:24 | RW   | DLY_RFTR_EN | Delay of RF_TR assertion | 0x0           |
| 23:16 | RW   | DLY_TRSW_EN | Delay of TR_SW assertion | 0x4           |
| 15:8  | RW   | DLY_PAPE_EN | Delay of PA_PE assertion | 0x8           |
| 7:0   | RW   | DLY_TXPE_EN | Delay of TX_PE assertion | 0xc           |

Note1: The timing unit is 0.25us.

Note2: SIFS\_TIME should compensate with DLY\_TXPE\_EN.

TX\_SW\_CFG1: (offset: 0x1334)

| Bits  | Type | Name         | Description                 | Initial value |
|-------|------|--------------|-----------------------------|---------------|
| 31:24 | -    | -            | Reserved                    | 0x0           |
| 23:16 | RW   | DLY_RFTR_DIS | Delay of RF_TR de-assertion | 0xc           |
| 15:8  | RW   | DLY_TRSW_DIS | Delay of TR_SW de-assertion | 0x8           |
| 7:0   | RW   | DLY_PAPE_DIS | Delay of PA_PE de-assertion | 0x8           |

Note1: The timing unit is 0.25us.

Note2: The delay is started from TX\_END event of BBP.

Note3: TX\_PE is de-asserted automatically as last data byte passed to BBP.

TX\_SW\_CFG2: (offset: 0x1338)

| Bits  | Type | Name        | Description                  | Initial value |
|-------|------|-------------|------------------------------|---------------|
| 31:24 | RW   | DLY_LNA_EN  | Delay of LNA* assertion      | 0x0           |
| 23:16 | RW   | DLY_LNA_DIS | Delay of LNA* de-assertion   | 0xc           |
| 15:8  | RW   | DLY_DAC_EN  | Delay of DAC_PE assertion    | 0x4           |
| 7:0   | RW   | DLY_DAC_DIS | Delay of DAC_PE de-assertion | 0x8           |

Note1: The timing unit is 0.25us.

Note 2: LNA\* includes LNA\_A0, LNA\_A1, LNA\_G0, LNA\_G1.

TXOP\_THRES\_CFG: (offset: 0x133c)

| Bits  | Type | Name           | Description                                                                                                                                                                                                   | Initial value |
|-------|------|----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:24 | RW   | TXOP_REM_THRES | Remaining TXOP threshold, unit: 32us<br>As the remaining TXOP is less than the threshold, the TXOP is passed silently.                                                                                        | 0x0           |
| 23:16 | RW   | CF_END_THRES   | CF-END threshold, unit: 32us<br>As the remaining TXOP is greater than the threshold, the CF-END will be send to release the remaining TXOP reserved by long NAV.<br>Set 0xFF to disable CF_END transmission.  | 0x0           |
| 15:8  | RW   | RDG_IN_THRES   | RX RDG threshold, unit: 32us<br>As the remaining TXOP (specified in the duration field of the RX frame with RDG=1) is greater than or equal to the threshold, the granted reverse direction TXOP may be used. | 0x0           |
| 7:0   | RW   | RDG_OUT_THRES  | TX RDG threshold, unit: 32us                                                                                                                                                                                  | 0x0           |

|  |  |  |                                                                                                         |  |
|--|--|--|---------------------------------------------------------------------------------------------------------|--|
|  |  |  | As the remaining TXOP is greater than or equal to the threshold, RDG in the TX frame may be set to one. |  |
|--|--|--|---------------------------------------------------------------------------------------------------------|--|

**TXOP\_CTRL\_CFG: (offset: 0x1340)**

| Bits  | Type | Name         | Description                                                                                                                                                                                                                                                                        | Initial value |
|-------|------|--------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:20 | -    | -            | Reserved                                                                                                                                                                                                                                                                           | 0x0           |
| 19:16 | RW   | EXT_CW_MIN   | Cwmin for extension channel backoff<br><br>When EXT_CCA_EN is enabled, 40Mhz transmission will be suppressed to 20Mhz if the extension CCA is busy or extension channel backoff is not finished.<br><br>Default: Cwmin=0, disable.                                                 | 0x0           |
| 15:8  | RW   | EXT_CCA_DLY  | Extension CCA signal delay time (unit: usec)<br><br>Create delayed version of extension CCA signal reference time for extension channel IFS.<br><br>Default: (ofdm SIFS) + (long slot time) = 16 + 20 = 36 (usec)                                                                  | 0x24          |
| 7     | RW   | EXT_CCA_EN   | Extension CCA reference enable<br><br>When transmit in 40Mhz mode, defer until extension CCA is also clear.<br><br>0: disable<br>1: enable                                                                                                                                         | 0x0           |
| 6     | RW   | LSIG_TXOP_EN | L-SIG TXOP protection enable<br><br>Extension of mix mode L-SIG protection range to following ACK/CTS.                                                                                                                                                                             | 0x0           |
| 5:0   | RW   | TXOP_TRUN_EN | TXOP truncation enable<br><br>Bit5: reserved<br>Bit4: truncation for MIMO power save RTS/CTS<br>Bit3: truncation for user TXOP mode<br>Bit2: truncation for TX rate group change<br>Bit1: truncation for AC change<br>Bit0: TXOP timeout truncation<br><br>0: disable<br>1: enable | 0x3f          |

**TX\_RTS\_CFG: (offset: 0x1344)**

| Bits  | Type | Name       | Description                | Initial value |
|-------|------|------------|----------------------------|---------------|
| 31:24 | -    | -          | Reserved                   | 0x0           |
| 24    | RW   | RTS_FBK_EN | RTS rate fallback enable   | 0x0           |
| 23:8  | RW   | RTS_THRES  | RTS threshold (unit: byte) | 0xffff        |



|     |    |               |                                                                                                                            |     |
|-----|----|---------------|----------------------------------------------------------------------------------------------------------------------------|-----|
|     |    |               | MPDU or AMPDU with length greater than RTS threshold will be protected with RTS/CTS exchange at the beginning of the TXOP. |     |
| 7:0 | RW | RTS_RTY_LIMIT | Auto RTS retry limit                                                                                                       | 0x7 |

## TX\_TIMEOUT\_CFG: (offset: 0x1348)

| Bits  | Type | Name           | Description                                                                                                                                                                                  | Initial value |
|-------|------|----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:24 | -    | -              | Reserved                                                                                                                                                                                     | 0x0           |
| 23:16 | RW   | TXOP_TIMEOUT   | TXOP timeout value for TXOP truncation<br><br>Unit: 1usec<br><br><b>Note:</b> It is recommended that (SLOT_TIME) > (TXOP_TIMEOUT) > (RX_ACK_TIMEOUT)<br>Default: For 20us long slot time.    | 0xf           |
| 15:8  | RW   | RX_ACK_TIMEOUT | RX ACK/CTS timeout value for TX procedure<br><br>Unit: 1usec<br><br><b>Note:</b> It is recommended that (SLOT_TIME) > (TXOP_TIMEOUT) > (RX_ACK_TIMEOUT)<br>Default: For 20us long slot time. | 0xa           |
| 7:4   | RW   | MPDU_LIFE_TIME | TX MPDU expiration time<br><br>Expiration time = $2^{(9+MPDU\_LIFE\_TIME)}$ us<br><br>Default value is $2^{(9+9)} \approx 256ms$                                                             | 0x9           |
| 3:0   | -    | -              | Reserved                                                                                                                                                                                     | 0x0           |

## TX\_RTY\_CFG: (offset: 0x134c)

| Bits  | Type | Name            | Description                                                                                        | Initial value |
|-------|------|-----------------|----------------------------------------------------------------------------------------------------|---------------|
| 31    | -    | -               | Reserved                                                                                           | 0x0           |
| 30    | RW   | TX_AUTOFB_EN    | TX retry PHY rate auto fallback enable<br><br>0: disable<br>1: enable                              | 0x0           |
| 29    | RW   | AGG_RTY_MODE    | Aggregate MPDU retry mode<br><br>0: expired by retry limit<br>1: expired by MPDU life timer        | 0x1           |
| 28    | RW   | NAG_RTY_MODE    | Non-aggregate MPDU retry mode<br><br>0: expired by retry limit<br>1: expired by MPDU life timer    | 0x0           |
| 27:16 | RW   | LONG_RTY_THRESH | Long retry threshold<br><br>MPDU with length over this threshold is applied with long retry limit. | 0xbb8         |

|      |    |                 |                   |     |
|------|----|-----------------|-------------------|-----|
| 15:8 | RW | LONG_RTY_LIMIT  | Long retry limit  | 0x4 |
| 7:0  | RW | SHORT_RTY_LIMIT | Short retry limit | 0x7 |

**TX\_LINK\_CFG: (offset: 0x1350)**

| Bits  | Type | Name                | Description                                                                                              | Initial value |
|-------|------|---------------------|----------------------------------------------------------------------------------------------------------|---------------|
| 31:24 | RO   | REMOTE_MFS          | Remote MCS feedback sequence number                                                                      | 0x7f          |
| 23:16 | RO   | REMOTE_MFB          | Remote MCS feedback                                                                                      | 0x7f          |
| 15:13 | -    | -                   | Reserved                                                                                                 | 0x0           |
| 12    | RW   | TX_CFACK_EN         | Piggyback CF-ACK enable<br>0: disable<br>1: enable                                                       | 0x0           |
| 11    | RW   | TX_RDG_EN           | RDG TX enable<br>0: disable<br>1: enable                                                                 | 0x0           |
| 10    | RW   | TX_MRQ_EN           | MCS request TX enable<br>0: disable<br>1: enable                                                         | 0x0           |
| 9     | RW   | REMOTE_UMFS_EN      | Remote un-solicit MFB enable<br>0: do not apply remote un-solicit MFB (MFS=7)<br>1: apply un-solicit MFB | 0x0           |
| 8     | RW   | TX_MFB_EN           | TX apply remote MFB<br>0: disable<br>1: enable                                                           | 0x0           |
| 7:0   | RW   | REMOTE_MFB_LITETIME | Remote MFB life time<br>Unit: 32us                                                                       | 0x20          |

**HT\_FBK\_CFG0: (offset: 0x1354)**

| Bits  | Type | Name        | Description                     | Initial value |
|-------|------|-------------|---------------------------------|---------------|
| 31:28 | RW   | HT_MCS7_FBK | Auto fall back MCS as HT MCS =7 | 0x6           |
| 27:24 | RW   | HT_MCS6_FBK | Auto fall back MCS as HT MCS =6 | 0x5           |
| 23:20 | RW   | HT_MCS5_FBK | Auto fall back MCS as HT MCS =5 | 0x4           |
| 19:16 | RW   | HT_MCS4_FBK | Auto fall back MCS as HT MCS =4 | 0x3           |
| 15:12 | RW   | HT_MCS3_FBK | Auto fall back MCS as HT MCS =3 | 0x2           |
| 11:8  | RW   | HT_MCS2_FBK | Auto fall back MCS as HT MCS =2 | 0x1           |
| 7:4   | RW   | HT_MCS1_FBK | Auto fall back MCS as HT MCS =1 | 0x0           |
| 3:0   | RW   | HT_MCS0_FBK | Auto fall back MCS as HT MCS =0 | 0x0           |

**HT\_FBK\_CFG1: (offset: 0x1358)**

| Bits  | Type | Name         | Description                      | Initial value |
|-------|------|--------------|----------------------------------|---------------|
| 31:28 | RW   | HT_MCS15_FBK | Auto fall back MCS as HT MCS =15 | 0xe           |

|       |    |              |                                  |     |
|-------|----|--------------|----------------------------------|-----|
| 27:24 | RW | HT_MCS14_FBK | Auto fall back MCS as HT MCS =14 | 0xd |
| 23:20 | RW | HT_MCS13_FBK | Auto fall back MCS as HT MCS =13 | 0xc |
| 19:16 | RW | HT_MCS12_FBK | Auto fall back MCS as HT MCS =12 | 0xb |
| 15:12 | RW | HT_MCS11_FBK | Auto fall back MCS as HT MCS =11 | 0xa |
| 11:8  | RW | HT_MCS10_FBK | Auto fall back MCS as HT MCS =10 | 0x9 |
| 7:4   | RW | HT_MCS9_FBK  | Auto fall back MCS as HT MCS =9  | 0x8 |
| 3:0   | RW | HT_MCS8_FBK  | Auto fall back MCS as HT MCS =8  | 0x8 |

Note1. The MCS is a fallback stopping state, as the fallback MCS is the same as current MCS.

Note2. HT TX PHY rates will not fallback to legacy PHY rates.

LG\_FBK\_CFG0: (offset: 0x135c)

| Bits  | Type | Name      | Description                                            | Initial value |
|-------|------|-----------|--------------------------------------------------------|---------------|
| 31:28 | RW   | OFDM7_FBK | Auto fall back MCS as previous TX rate is OFDM 54Mbps. | 0xe           |
| 27:24 | RW   | OFDM6_FBK | Auto fall back MCS as previous TX rate is OFDM 48Mbps. | 0xd           |
| 23:20 | RW   | OFDM5_FBK | Auto fall back MCS as previous TX rate is OFDM 36Mbps. | 0xc           |
| 19:16 | RW   | OFDM4_FBK | Auto fall back MCS as previous TX rate is OFDM 24Mbps. | 0xb           |
| 15:12 | RW   | OFDM3_FBK | Auto fall back MCS as previous TX rate is OFDM 18Mbps. | 0xa           |
| 11:8  | RW   | OFDM2_FBK | Auto fall back MCS as previous TX rate is OFDM 12Mbps. | 0x9           |
| 7:4   | RW   | OFDM1_FBK | Auto fall back MCS as previous TX rate is OFDM 9Mbps.  | 0x8           |
| 3:0   | RW   | OFDM0_FBK | Auto fall back MCS as previous TX rate is OFDM 6Mbps.  | 0x8           |

LG\_FBK\_CFG1: (offset: 0x1360)

| Bits  | Type | Name     | Description                                            | Initial value |
|-------|------|----------|--------------------------------------------------------|---------------|
| 31:16 | -    | -        | Reserved                                               | 0x0           |
| 15:12 | RW   | CCK3_FBK | Auto fall back MCS as previous TX rate is CCK 11Mbps.  | 0x2           |
| 11:8  | RW   | CCK2_FBK | Auto fall back MCS as previous TX rate is CCK 5.5Mbps. | 0x1           |
| 7:4   | RW   | CCK1_FBK | Auto fall back MCS as previous TX rate is CCK 2Mbps.   | 0x0           |
| 3:0   | RW   | CCK0_FBK | Auto fall back MCS as previous TX rate is CCK 1Mbps.   | 0x0           |

Note1. Bit3 of each legacy fallback rate is selection of OFDM/CCK. 0=CCK, 1=OFDM.

CCK\_PROT\_CFG: (offset: 0x1364)

| Bits  | Type | Name               | Description                                                                                                                                                                                      | Initial value |
|-------|------|--------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:27 | -    | -                  | Reserved                                                                                                                                                                                         | 0x0           |
| 26    | RW   | CCK_RTSTH_EN       | RTS threshold enable on CCK TX<br>0: disable<br>1: enable                                                                                                                                        | 0x0           |
| 25:20 | RW   | CCK_TXOP_ALLO<br>W | CCK TXOP allowance<br>(0: disallow, 1: allow)<br>Bit25: allow GF-40 TX<br>Bit24: allow GF-20 TX<br>Bit23: allow MM-40 TX<br>Bit22: allow MM-20 TX<br>Bit21: allow OFDM TX<br>Bit20: allow CCK TX | 0x1           |
| 19:18 | RW   | CCK_PROT_NAV       | TXOP protection type for CCK TX<br>0: None<br>1: Short NAV protection<br>2: Long NAV protection                                                                                                  | 0x0           |

|       |    |               |                                                                                                           |     |
|-------|----|---------------|-----------------------------------------------------------------------------------------------------------|-----|
|       |    |               | 3: Reserved (None)                                                                                        |     |
| 17:16 | RW | CCK_PROT_CTRL | Protection control frame type for CCK TX<br>0: None<br>1: RTS/CTS<br>2: CTS-to-self<br>3: Reserved (None) | 0x0 |
| 15:0  | RW | CCK_PROT_RATE | Protection control frame rate for CCK TX<br>(Including RTS/CTS-to-self/CF-END)<br>Default: CCK 11M        | 0x3 |

**OFDM\_PROT\_CFG: (offset: 0x1368)**

| Bits  | Type | Name               | Description                                                                                                                                                                                       | Initial value |
|-------|------|--------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:27 | -    | -                  | Reserved                                                                                                                                                                                          | 0x0           |
| 26    | RW   | OFDM_RTSTH_EN      | RTS threshold enable on OFDM TX<br>0: disable<br>1: enable                                                                                                                                        | 0x0           |
| 25:20 | RW   | OFDM_PROT_TX<br>OP | OFDM TXOP allowance<br>(0: disallow, 1: allow)<br>Bit25: allow GF-40 TX<br>Bit24: allow GF-20 TX<br>Bit23: allow MM-40 TX<br>Bit22: allow MM-20 TX<br>Bit21: allow OFDM TX<br>Bit20: allow CCK TX | 0x2           |
| 19:18 | RW   | OFDM_PROT_NA<br>V  | TXOP protection type for OFDM TX<br>0: None<br>1: Short NAV protection<br>2: Long NAV protection<br>3: Reserved (None)                                                                            | 0x0           |
| 17:16 | RW   | OFDM_PROT_CT<br>RL | Protection control frame type for OFDM TX<br>0: None<br>1: RTS/CTS<br>2: CTS-to-self<br>3: Reserved (None)                                                                                        | 0x0           |
| 15:0  | RW   | OFDM_PROT_RA<br>TE | Protection control frame rate for OFDM TX<br>(Including RTS/CTS-to-self/CF-END)<br>Default: CCK 11M                                                                                               | 0x3           |

**MM20\_PROT\_CFG: (offset: 0x136c)**

| Bits  | Type | Name               | Description                                                                                                               | Initial value |
|-------|------|--------------------|---------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:27 | -    | -                  | Reserved                                                                                                                  | 0x0           |
| 26    | RW   | MM20_RTSTH_EN      | RTS threshold enable on MM20 TX<br>0: disable<br>1: enable                                                                | 0x0           |
| 25:20 | RW   | MM20_PROT_TXO<br>P | MM20 TXOP allowance<br>(0: disallow, 1: allow)<br>Bit25: allow GF-40 TX<br>Bit24: allow GF-20 TX<br>Bit23: allow MM-40 TX | 0x4           |

|       |    |                |                                                                                                                        |        |
|-------|----|----------------|------------------------------------------------------------------------------------------------------------------------|--------|
|       |    |                | Bit22: allow MM-20 TX<br>Bit21: allow OFDM TX<br>Bit20: allow CCK TX                                                   |        |
| 19:18 | RW | MM20_PROT_NAV  | TXOP protection type for MM20 TX<br>0: None<br>1: Short NAV protection<br>2: Long NAV protection<br>3: Reserved (None) | 0x0    |
| 17:16 | RW | MM20_PROT_CTRL | Protection control frame type for MM20 TX<br>0: None<br>1: RTS/CTS<br>2: CTS-to-self<br>3: Reserved (None)             | 0x0    |
| 15:0  | RW | MM20_PROT_RATE | Protection control frame rate for MM20 TX<br>(Including RTS/CTS-to-self/CF-END)<br>Default: OFDM 24M                   | 0x4004 |

**MM40\_PROT\_CFG: (offset: 0x1370)**

| Bits  | Type | Name           | Description                                                                                                                                                                                       | Initial value |
|-------|------|----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:27 | -    | -              | Reserved                                                                                                                                                                                          | 0x0           |
| 26    | RW   | MM40_RTSTH_EN  | RTS threshold enable on MM40 TX<br>0: disable<br>1: enable                                                                                                                                        | 0x0           |
| 25:20 | RW   | MM40_PROT_TXOP | MM40 TXOP allowance<br>(0: disallow, 1: allow)<br>Bit25: allow GF-40 TX<br>Bit24: allow GF-20 TX<br>Bit23: allow MM-40 TX<br>Bit22: allow MM-20 TX<br>Bit21: allow OFDM TX<br>Bit20: allow CCK TX | 0x8           |
| 19:18 | RW   | MM40_PROT_NAV  | TXOP protection type for MM40 TX<br>0: None<br>1: Short NAV protection<br>2: Long NAV protection<br>3: Reserved (None)                                                                            | 0x0           |
| 17:16 | RW   | MM40_PROT_CTRL | Protection control frame type for MM40 TX<br>0: None<br>1: RTS/CTS<br>2: CTS-to-self<br>3: Reserved (None)                                                                                        | 0x0           |
| 15:0  | RW   | MM40_PROT_RATE | Protection control frame rate for MM40 TX<br>(Including RTS/CTS-to-self/CF-END)<br>Default: duplicate OFDM 24M                                                                                    | 0x4084        |

**GF20\_PROT\_CFG: (offset: 0x1374)**

| Bits  | Type | Name          | Description                     | Initial value |
|-------|------|---------------|---------------------------------|---------------|
| 31:27 | -    | -             | Reserved                        | 0x0           |
| 26    | RW   | GF20_RTSTH_EN | RTS threshold enable on GF20 TX | 0x0           |

|       |    |                    |                                                                                                                                                                                                   |        |
|-------|----|--------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|
|       |    |                    | 0: disable<br>1: enable                                                                                                                                                                           |        |
| 25:20 | RW | GF20_PROT_TX<br>OP | GF20 TXOP allowance<br>(0: disallow, 1: allow)<br>Bit25: allow GF-40 TX<br>Bit24: allow GF-20 TX<br>Bit23: allow MM-40 TX<br>Bit22: allow MM-20 TX<br>Bit21: allow OFDM TX<br>Bit20: allow CCK TX | 0x10   |
| 19:18 | RW | GF20_PROT_NA<br>V  | TXOP protection type for GF20 TX<br>0: None<br>1: Short NAV protection<br>2: Long NAV protection<br>3: Reserved (None)                                                                            | 0x0    |
| 17:16 | RW | GF20_PROT_CTR<br>L | Protection control frame type for GF20 TX<br>0: None<br>1: RTS/CTS<br>2: CTS-to-self<br>3: Reserved (None)                                                                                        | 0x0    |
| 15:0  | RW | GF20_PROT_RAT<br>E | Protection control frame rate for GF20 TX<br>(Including RTS/CTS-to-self/CF-END)<br>Default: OFDM 24M                                                                                              | 0x4004 |

**GF40\_PROT\_CFG: (offset: 0x1378)**

| Bits  | Type | Name               | Description                                                                                                                                                                                       | Initial value |
|-------|------|--------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:27 | -    | -                  | Reserved                                                                                                                                                                                          | 0x0           |
| 26    | RW   | GF40_RTSTH_EN      | RTS threshold enable on GF40 TX<br>0: disable<br>1: enable                                                                                                                                        | 0x0           |
| 25:20 | RW   | GF40_PROT_TX<br>OP | GF40 TXOP allowance<br>(0: disallow, 1: allow)<br>Bit25: allow GF-40 TX<br>Bit24: allow GF-20 TX<br>Bit23: allow MM-40 TX<br>Bit22: allow MM-20 TX<br>Bit21: allow OFDM TX<br>Bit20: allow CCK TX | 0x10          |
| 19:18 | RW   | GF40_PROT_NA<br>V  | TXOP protection type for GF40 TX<br>0: None<br>1: Short NAV protection<br>2: Long NAV protection<br>3: Reserved (None)                                                                            | 0x0           |
| 17:16 | RW   | GF40_PROT_CTR<br>L | Protection control frame type for GF40 TX<br>0: None<br>1: RTS/CTS<br>2: CTS-to-self<br>3: Reserved (None)                                                                                        | 0x0           |
| 15:0  | RW   | GF40_PROT_RAT      | Protection control frame rate for GF40 TX                                                                                                                                                         | 0x4084        |

|  |  |   |                                                                   |  |
|--|--|---|-------------------------------------------------------------------|--|
|  |  | E | (Including RTS/CTS-to-self/CF-END)<br>Default: duplicate OFDM 24M |  |
|--|--|---|-------------------------------------------------------------------|--|

EXP\_CTS\_TIME: (offset: 0x137c)

| Bits  | Type | Name              | Description                                                                                                    | Initial value |
|-------|------|-------------------|----------------------------------------------------------------------------------------------------------------|---------------|
| 31    | -    | -                 | Reserved                                                                                                       | 0x0           |
| 30:16 | RW   | EXP_OFDM_CTS_TIME | Expected time for OFDM CTS response (unit: 1us)<br>Used for outgoing NAV setting.<br>Default: SIFS + 6Mbps CTS | 0x38          |
| 15    | RO   | -                 | Reserved                                                                                                       | 0x0           |
| 14:0  | RW   | EXP_CCK_CTS_TIME  | Expected time for CCK CTS response (unit: 1us)<br>Used for outgoing NAV setting.<br>Default: SIFS + 1Mbps CTS  | 0x13a         |

EXP\_ACK\_TIME: (offset: 0x1380)

| Bits  | Type | Name              | Description                                                                                                             | Initial value |
|-------|------|-------------------|-------------------------------------------------------------------------------------------------------------------------|---------------|
| 31    | -    | -                 | Reserved                                                                                                                | 0x0           |
| 30:16 | RW   | EXP_OFDM_ACK_TIME | Expected time for OFDM ACK response (unit: 1us)<br>Used for outgoing NAV setting.<br>Default: SIFS + 6Mbps ACK preamble | 0x24          |
| 15    | -    | -                 | Reserved                                                                                                                | 0x0           |
| 14:0  | RW   | EXP_CCK_ACK_TIME  | Expected time for OFDM ACK response (unit: 1us)<br>Used for outgoing NAV setting.<br>Default: SIFS + 1Mbps ACK preamble | 0xca          |

#### 5.17.5.4 MAC RX configuration registers

RX\_FILTER\_CFG: (offset: 0x1400)

| Bits  | Type | Name          | Description                  | Initial value |
|-------|------|---------------|------------------------------|---------------|
| 31:17 | -    | -             | Reserved                     | 0x0           |
| 16    | RW   | DROP_CTRL_RSV | Drop reserve control subtype | 0x1           |
| 15    | RW   | DROP_BAR      | Drop BAR                     | 0x0           |
| 14    | RW   | DROP_BA       | Drop BA                      | 0x1           |
| 13    | RW   | DROP_PSPOLL   | Drop PS-Poll                 | 0x0           |
| 12    | RW   | DROP_RTS      | Drop RTS                     | 0x1           |
| 11    | RW   | DROP_CTS      | Drop CTS                     | 0x1           |
| 10    | RW   | DROP_ACK      | Drop ACK                     | 0x1           |
| 9     | RW   | DROP_CFEND    | Drop CF-END                  | 0x1           |
| 8     | RW   | DROP_CFACK    | Drop CF-END + CF-ACK         | 0x1           |
| 7     | RW   | DROP_DUPL     | Drop duplicated frame        | 0x1           |

|   |    |                 |                                 |     |
|---|----|-----------------|---------------------------------|-----|
| 6 | RW | DROP_BC         | Drop broadcast frame            | 0x0 |
| 5 | RW | DROP_MC         | Drop multicast frame            | 0x0 |
| 4 | RW | DROP_VER_ERR    | Drop 802.11 version error frame | 0x1 |
| 3 | RW | DROP_NOT_MY_BSS | Drop frame that is not my BSSID | 0x1 |
| 2 | RW | DROP_UC_NOM E   | Drop not to me unicast frame    | 0x1 |
| 1 | RW | DROP_PHY_ERR    | Drop physical error frame       | 0x1 |
| 0 | RW | DROP_CRC_ERR    | Drop CRC error frame            | 0x1 |

Note: 1: enable, 0: disable.

AUTO\_RSP\_CFG: (offset: 0x1404)

| Bits | Type | Name             | Description                                                                                                                               | Initial value |
|------|------|------------------|-------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:8 | -    | -                | Reserved                                                                                                                                  | 0x0           |
| 7    | RW   | CTRL_PWR_BIT     | Power bit value in control frame                                                                                                          | 0x0           |
| 6    | RW   | BAC_ACK_POLICY   | BA frame -> BAC -> Ack policy bit value                                                                                                   | 0x0           |
| 5    | -    | -                | Reserved                                                                                                                                  | 0x0           |
| 4    | RW   | CCK_SHORT_EN     | CCK short preamble auto response enable<br>0: disable<br>1: enable                                                                        | 0x0           |
| 3    | RW   | CTS_40M_REF      | In duplicate legacy CTS response mode, refer to extension CCA to decide duplicate or not.<br>0: disable<br>1: enable                      | 0x0           |
| 2    | RW   | CTS_40M_MODE     | Duplicate legacy CTS response mode<br>0: disable<br>1: enable                                                                             | 0x0           |
| 1    | RW   | BAC_ACKPOLICY_EN | BAC ACK policy bit enable<br>0: disable; don't care this bit<br>1: enable; no BA auto responding upon reception of BAR with no ACK policy | 0x1           |
| 0    | RW   | AUTO_RSP_EN      | Auto responder enable                                                                                                                     | 0x1           |

LEGACY\_BASIC\_RATE: (offset: 0x1408)

| Bits  | Type | Name              | Description                                                                                                                                                                                                           | Initial value |
|-------|------|-------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:12 | -    | -                 | Reserved                                                                                                                                                                                                              | 0x0           |
| 11:0  | RW   | LEGACY_BASIC_RATE | Legacy basic rate bit mask<br><br>Bit0: 1 Mbps is basic rate<br>Bit1: 2 Mbps is basic rate<br>Bit2: 5.5 Mbps is basic rate<br>Bit3: 11 Mbps is basic rate<br>Bit4: 6 Mbps is basic rate<br>Bit5: 9 Mbps is basic rate | 0x0           |



|  |  |  |                                                                                                                                                                                                                         |  |
|--|--|--|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|
|  |  |  | Bit6: 12 Mbps is basic rate<br>Bit7: 18 Mbps is basic rate<br>Bit8: 24 Mbps is basic rate<br>Bit9: 36 Mbps is basic rate<br>Bit10: 48 Mbps is basic rate<br>Bit11: 54 Mbps is basic rate<br><br>0: disable<br>1: enable |  |
|--|--|--|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|

**HT\_BASIC\_RATE: (offset: 0x140c)**

| Bits  | Type | Name          | Description                                                                          | Initial value |
|-------|------|---------------|--------------------------------------------------------------------------------------|---------------|
| 31:16 | RW   | -             | Reserved                                                                             | 0x0           |
| 15:0  | RW   | HT_BASIC_RATE | HT basic rate for auto responding control frame<br><br>Bit15 =1, enable MCS feedback | 0x0           |

**HT\_CTRL\_CFG: (offset: 0x1410)**

| Bits | Type | Name          | Description                                                                     | Initial value |
|------|------|---------------|---------------------------------------------------------------------------------|---------------|
| 31:9 | -    | -             | Reserved                                                                        | 0x0           |
| 8:0  | RW   | HT_CTRL_THRES | Remaining TXOP threshold for HT control frame auto responding<br><br>(unit: us) | 0x100         |

**SIFS\_COST\_CFG: (offset: 0x1414)**

| Bits  | Type | Name           | Description                                                 | Initial value |
|-------|------|----------------|-------------------------------------------------------------|---------------|
| 31:16 | -    | -              | Reserved                                                    | 0x0           |
| 15:8  | RW   | OFDM_SIFS_COST | OFDM SIFS time (unit: 1us)<br><br>Applied after OFDM TX/RX. | 0x10          |
| 7:0   | RW   | CCK_SIFS_COST  | CCK SIFS time (unit: 1us)<br><br>Applied after CCK TX/RX.   | 0xa           |

**Note:** The OFDM\_SIFS\_COST and CCK\_SIFS\_COST are used only for duration field calculation. It will not affect the responding timing.

**RX\_PARSER\_CFG: (offset: 0x1418)**

| Bits  | Type | Name       | Description                                                                                               | Initial value |
|-------|------|------------|-----------------------------------------------------------------------------------------------------------|---------------|
| 31:16 | -    | -          | Reserved                                                                                                  | 0x0           |
| 0     | RW   | NAV_ALL_EN | Set NAV for all received frames<br><br>0: disable (unicast to me frame will not set the NAV)<br>1: enable | 0x0           |

**5.17.5.5 MAC Security Configuration Registers**
**TX\_SEC\_CNT0: (offset: 0x1500)**

| Bits | Type | Name | Description | Initial value |
|------|------|------|-------------|---------------|
|------|------|------|-------------|---------------|

|       |    |                    |                              |     |
|-------|----|--------------------|------------------------------|-----|
| 31:16 | RC | TX_SEC_ERR_CN<br>T | TX SEC packet error count    | 0x0 |
| 15:0  | RC | TX_SEC_CPL_CN<br>T | TX SEC packet complete count | 0x0 |

RX\_SEC\_CNT0: (offset: 0x1504)

| Bits  | Type | Name               | Description                  | Initial value |
|-------|------|--------------------|------------------------------|---------------|
| 31:16 | -    | -                  | Reserved                     | 0x0           |
| 15:0  | RC   | RX_SEC_CPL_CN<br>T | RX SEC packet complete count | 0x0           |

CCMP\_FC\_MUTE: (offset: 0x1508)

| Bits  | Type | Name                | Description              | Initial value |
|-------|------|---------------------|--------------------------|---------------|
| 31:16 | RW   | HT_CCMP_FC_M<br>UTE | HT rate CCMP FC mute     | 0xc78f        |
| 15:0  | RW   | LG_CCMP_FC_M<br>UTE | Legacy rate CCMP FC mute | 0xc78f        |

#### 5.17.5.6 MAC HCCA/PSMP CSR

TXOP\_HLDR\_ADDR0: (offset: 0x1600)

| Bits  | Type | Name       | Description                   | Initial value |
|-------|------|------------|-------------------------------|---------------|
| 31:24 | RW   | TXOP_HOL_3 | TXOP holder MAC address byte3 | 0x0           |
| 23:16 | RW   | TXOP_HOL_2 | TXOP holder MAC address byte2 | 0x0           |
| 15:8  | RW   | TXOP_HOL_1 | TXOP holder MAC address byte1 | 0x0           |
| 7:0   | RW   | TXOP_HOL_0 | TXOP holder MAC address byte0 | 0x0           |

TXOP\_HLDR\_ADDR1: (offset: 0x1604)

| Bits  | Type | Name       | Description                   | Initial value |
|-------|------|------------|-------------------------------|---------------|
| 31:16 | -    | -          | Reserved                      | 0x0           |
| 15:8  | RW   | TXOP_HOL_5 | TXOP holder MAC address byte5 | 0x0           |
| 7:0   | RW   | TXOP_HOL_4 | TXOP holder MAC address byte4 | 0x0           |

**Note:** Byte0 is the first byte on network. Its LSB bit is the first bit on network. For a MAC address captured on the network with order 00:01:02:03:04:05, byte0=00, byte1=01 etc.

TXOP\_HLDR\_ET: (offset: 0x1608)

| Bits  | Type | Name         | Description                                                                                                                                                                                                                                                                          | Initial value |
|-------|------|--------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:26 | -    | -            | Reserved                                                                                                                                                                                                                                                                             | 0x0           |
| 25    | RW   | TXOP_ETM1_EN | TXOP holder early termination interrupt enable (Type 1)<br><br>Upon the reception of QoS data frame from TXOP_HLDR_ADDR (A2) and Queue size (QS) in QOS control field (QC) is equal to zero, "TXOP holder early termination interrupt" will be issue.<br><br>0: disable<br>1: enable | 0x0           |
| 24    | RW   | TXOP_ETM0_EN | TXOP holder early termination interrupt enable (Type 0)<br><br>When RX packet is from TXOP holder specified in                                                                                                                                                                       | 0x0           |

|       |    |                |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |     |
|-------|----|----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|
|       |    |                | <p>QOS_CSR0,1 (match with Addr2) and duration value is less than or equal to early termination duration threshold specified below, "TXOP holder early termination" interrupt will be issued after CRC check is ok.</p> <p>Upon the reception of QoS data frame from TXOP_HLDR_ADDR (A2) and Duration (DUR) is less than or equal to early termination duration threshold (TXOP_ETM_THRES), "TXOP holder early termination interrupt" will be issue.</p> <p>0: disable<br/>1: enable</p> |     |
| 23:16 | RW | TXOP_ETM_THRES | <p>TXOP early termination duration threshold</p> <p>Unit: 1usec</p>                                                                                                                                                                                                                                                                                                                                                                                                                     | 0x0 |
| 15:9  | -  | -              | Reserved                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | 0x0 |
| 8     | WC | TXOP_ETO_EN    | <p>TXOP holder early timeout enable</p> <p>Write 1 to enable early timeout check. (interrupt when timeout)</p> <p>When enabled, hardware will expect CCA event. If hardware didn't sense CCA over the TXOP holder early timeout threshold (TXOP_ETO_THRES), the "TXOP holder early timeout interrupt" will then be issued.</p>                                                                                                                                                          | 0x0 |
| 7:1   | RW | TXOP_ETO_THRES | <p>TXOP holder early timeout threshold</p> <p>Unit: 1usec</p>                                                                                                                                                                                                                                                                                                                                                                                                                           | 0x0 |
| 0     | RW | PER_RX_RST_EN  | <p>Baseband RX_PE per RX reset enable</p> <p>0: disable, 1: enable</p>                                                                                                                                                                                                                                                                                                                                                                                                                  | 0x0 |

**Note1:** TXOP holder early timeout interrupt (TXOP\_ETO\_INT) is used by AP for HC purpose.

**Note2:** TXOP holder early termination interrupt (TXOP\_ETM\_INT) is used by STA (both AP and non-AP STA) for HC purpose.

QOS\_CFPOLL\_RA\_DW0: (offset: 0x160c)

| Bits  | Type | Name            | Description                                        | Initial value |
|-------|------|-----------------|----------------------------------------------------|---------------|
| 31:24 | RO   | CFPOLL_A1_BYTE3 | Byte3 of A1 of received QoS Data (+) CF-Poll frame | 0x0           |
| 23:16 | RO   | CFPOLL_A1_BYTE2 | Byte2 of A1 of received QoS Data (+) CF-Poll frame | 0x0           |
| 15:8  | RO   | CFPOLL_A1_BYTE1 | Byte1 of A1 of received QoS Data (+) CF-Poll frame | 0x0           |
| 7:0   | RO   | CFPOLL_A1_BYTE0 | Byte0 of A1 of received QoS Data (+) CF-Poll frame | 0x0           |

QOS\_CFPOLL\_A1\_DW1: (offset: 0x1610)

| Bits  | Type | Name          | Description          | Initial value |
|-------|------|---------------|----------------------|---------------|
| 31:24 | -    | -             | Reserved             | 0x0           |
| 16    | RO   | CFPOLL_A1_TOM | 1: QoS CF-Poll to me | 0x0           |

|      |    |                  |                                                    |     |
|------|----|------------------|----------------------------------------------------|-----|
|      |    | E                | 0: Qos CF-Poll not to me                           |     |
| 15:8 | RO | CFPOLL_A1_BYTE 5 | Byte5 of A1 of received QoS Data (+) CF-Poll frame | 0x0 |
| 7:0  | RO | CFPOLL_A1_BYTE 4 | Byte4 of A1 of received QoS Data (+) CF-Poll frame | 0x0 |

QOS\_CFPOLL\_QC: (offset: 0x1614)

| Bits  | Type | Name             | Description                                        | Initial value |
|-------|------|------------------|----------------------------------------------------|---------------|
| 31:24 | -    | -                | Reserved                                           | 0x0           |
| 15:8  | RO   | CFPOLL_QC_BYTE 1 | Byte1 of QC of received QoS Data (+) CF-Poll frame | 0x0           |
| 7:0   | RO   | CFPOLL_QC_BYTE 0 | Byte0 of QC of received QoS Data (+) CF-Poll frame | 0x0           |

**Note:** CFPOLL\_RA\_DW0, CFPOLL\_RA\_DW1, and CFPOLL\_QC are updated after the reception of QoS Data (+) CF-Poll frame and RX QoS CF-Poll interrupt (RX\_QOS\_CFPOLL\_INT) is launched then.

#### 5.17.5.6 MAC Statistic Counters

RX\_STA\_CNT0: (offset: 0x1700)

| Bits  | Type | Name       | Description              | Initial value |
|-------|------|------------|--------------------------|---------------|
| 31:16 | RC   | PHY_ERRCNT | RX PHY error frame count | 0x0           |
| 15:0  | RC   | CRC_ERRCNT | RX CRC error frame count | 0x0           |

**Note1:** RX PHY error means PSDU length is shorter than indicated by PLCP.

**Note2:** RX PHY error is also treated as CRC error.

RX\_STA\_CNT1: (offset: 0x1704)

| Bits  | Type | Name        | Description           | Initial value |
|-------|------|-------------|-----------------------|---------------|
| 31:16 | RC   | PLPC_ERRCNT | RX PLCP error count   | 0x0           |
| 15:0  | RC   | CCA_ERRCNT  | CCA false alarm count | 0x0           |

**Note1:** CCA false alarm means there is no PLCP after CCA indication.

**Note2:** RX PLCP error means there is no PSDU after PLCP indication.

RX\_STA\_CNT2: (offset: 0x1708)

| Bits  | Type | Name        | Description                        | Initial value |
|-------|------|-------------|------------------------------------|---------------|
| 31:16 | RC   | RX_OVFL_CNT | RX FIFO overflow frame count       | 0x0           |
| 15:0  | RC   | RX_DUPL_CNT | RX duplicated filtered frame count | 0x0           |

**Note:** MAC will NOT auto respond ACK/BA to the frame originator when frame is lost due to RXFIFO overflow. However, MAC will respond when frame is duplicated filtered.

TX\_STA\_CNT0: (offset: 0x170c)

| Bits  | Type | Name        | Description     | Initial value |
|-------|------|-------------|-----------------|---------------|
| 31:16 | RC   | TX_BCN_CNT  | TX beacon count | 0x0           |
| 15:0  | RC   | TX_FAIL_CNT | Failed TX count | 0x0           |

TX\_STA\_CNT1: (offset: 0x1710)

| Bits  | Type | Name        | Description             | Initial value |
|-------|------|-------------|-------------------------|---------------|
| 31:16 | RC   | TX_RTY_CNT  | TX retransmission count | 0x0           |
| 15:0  | RC   | TX_SUCC_CNT | Successful TX count     | 0x0           |

TX\_STA\_CNT2: (offset: 0x1714)

| Bits  | Type | Name        | Description                | Initial value |
|-------|------|-------------|----------------------------|---------------|
| 31:16 | RC   | TX_UDFL_CNT | TX underflow count         | 0x0           |
| 15:0  | RC   | TX_ZERO_CNT | TX zero length frame count | 0x0           |

TX\_STAT\_FIFO: (offset: 0x1718)

| Bits  | Type | Name       | Description                                               | Initial value |
|-------|------|------------|-----------------------------------------------------------|---------------|
| 31:16 | RO   | TXQ_RATE   | TX success rate                                           | 0x0           |
| 15:8  | RO   | TXQ_WCID   | TX WCID                                                   | 0x0           |
| 7     | RO   | TXQ_ACKREQ | TX acknowledge required<br>0: not required<br>1: required | 0x0           |
| 6     | RO   | TXQ_AGG    | TX aggregate<br>0: non-aggregated<br>1: aggregated        | 0x0           |
| 5     | RO   | TXQ_OK     | TX success<br>0: failed<br>1: success                     | 0x0           |
| 4:1   | RO   | TXQ_PID    | TX Packet ID (Latched from TXWI)                          | 0x0           |
| 0     | RC   | TXQ_VLD    | TX status queue valid<br>0: queue empty, 1: valid         | 0x0           |

**Note:** TX status FIFO size = 16.

TX\_NAG\_AGG\_CNT: (offset: 0x171c)

| Bits  | Type | Name       | Description            | Initial value |
|-------|------|------------|------------------------|---------------|
| 31:16 | RC   | TX_AGG_CNT | Aggregate TX count     | 0x0           |
| 15:0  | RC   | TX_NAG_CNT | Non-aggregate TX count | 0x0           |

TX\_AGG\_CNT0: (offset: 0x1720)

| Bits  | Type | Name         | Description                   | Initial value |
|-------|------|--------------|-------------------------------|---------------|
| 31:16 | RC   | TX_AGG_2_CNT | Aggregate Size = 2 MPDU count | 0x0           |
| 15:0  | RC   | TX_AGG_1_CNT | Aggregate Size = 1 MPDU count | 0x0           |

TX\_AGG\_CNT1: (offset: 0x1724)

| Bits  | Type | Name         | Description                   | Initial value |
|-------|------|--------------|-------------------------------|---------------|
| 31:16 | RC   | TX_AGG_4_CNT | Aggregate Size = 4 MPDU count | 0x0           |
| 15:0  | RC   | TX_AGG_3_CNT | Aggregate Size = 3 MPDU count | 0x0           |

TX\_AGG\_CNT2: (offset: 0x1728)

| Bits  | Type | Name         | Description                   | Initial value |
|-------|------|--------------|-------------------------------|---------------|
| 31:16 | RC   | TX_AGG_6_CNT | Aggregate Size = 6 MPDU count | 0x0           |
| 15:0  | RC   | TX_AGG_5_CNT | Aggregate Size = 5 MPDU count | 0x0           |

TX\_AGG\_CNT3: (offset: 0x172c)

| Bits  | Type | Name         | Description                   | Initial value |
|-------|------|--------------|-------------------------------|---------------|
| 31:16 | RC   | TX_AGG_8_CNT | Aggregate Size = 8 MPDU count | 0x0           |
| 15:0  | RC   | TX_AGG_7_CNT | Aggregate Size = 7 MPDU count | 0x0           |

TX\_AGG\_CNT4: (offset: 0x1730)

| Bits  | Type | Name          | Description                    | Initial value |
|-------|------|---------------|--------------------------------|---------------|
| 31:16 | RC   | TX_AGG_10_CNT | Aggregate Size = 10 MPDU count | 0x0           |
| 15:0  | RC   | TX_AGG_9_CNT  | Aggregate Size = 9 MPDU count  | 0x0           |

TX\_AGG\_CNT5: (offset: 0x1734)

| Bits  | Type | Name          | Description                    | Initial value |
|-------|------|---------------|--------------------------------|---------------|
| 31:16 | RC   | TX_AGG_12_CNT | Aggregate Size = 12 MPDU count | 0x0           |
| 15:0  | RC   | TX_AGG_11_CNT | Aggregate Size = 11 MPDU count | 0x0           |

TX\_AGG\_CNT6: (offset: 0x1738)

| Bits  | Type | Name          | Description                    | Initial value |
|-------|------|---------------|--------------------------------|---------------|
| 31:16 | RC   | TX_AGG_14_CNT | Aggregate Size = 14 MPDU count | 0x0           |
| 15:0  | RC   | TX_AGG_13_CNT | Aggregate Size = 13 MPDU count | 0x0           |

TX\_AGG\_CNT7: (offset: 0x173c)

| Bits  | Type | Name          | Description                    | Initial value |
|-------|------|---------------|--------------------------------|---------------|
| 31:16 | RC   | TX_AGG_16_CNT | Aggregate Size > 16 MPDU count | 0x0           |
| 15:0  | RC   | TX_AGG_15_CNT | Aggregate Size = 15 MPDU count | 0x0           |

MPDU\_DENSITY\_CNT: (offset: 0x1740)

| Bits  | Type | Name            | Description                    | Initial value |
|-------|------|-----------------|--------------------------------|---------------|
| 31:16 | RC   | RX_ZERO_DEL_CNT | RX zero length delimiter count | 0x0           |
| 15:0  | RC   | TX_ZERO_DEL_CNT | TX zero length delimiter count | 0x0           |

### 3.3.1.4 MAC search table (base: 0x1018\_0000, offset: 0x1800)

RX WCID search entry format (8 bytes)

| Offset | Type | Name          | Description                                               | Initial value |
|--------|------|---------------|-----------------------------------------------------------|---------------|
| 0x00   | RW   | WC_MAC_ADDR0  | Client MAC address byte0                                  | 0x0           |
| 0x01   | RW   | WC_MAC_ADDR1  | Client MAC address byte1                                  | 0x0           |
| 0x02   | RW   | WC_MAC_ADDR2  | Client MAC address byte2                                  | 0x0           |
| 0x03   | RW   | WC_MAC_ADDR3  | Client MAC address byte3                                  | 0x0           |
| 0x04   | RW   | WC_MAC_ADDR4  | Client MAC address byte4                                  | 0x0           |
| 0x05   | RW   | WC_MAC_ADDR5  | Client MAC address byte5                                  | 0x0           |
| 0x06   | RW   | BA_SESS_MASK0 | BA session mask (lower)<br>Bit0 for TID0<br>Bit7 for TID7 | 0x0           |
| 0x07   | RW   | BA_SESS_MASK1 | BA session mask (upper)<br>Bit8 for TID8                  | 0x0           |

|  |  |  |                 |  |
|--|--|--|-----------------|--|
|  |  |  | Bit15 for TID15 |  |
|--|--|--|-----------------|--|

RX WCID search table (offset:0x1800)

| Offset | Type | Name             | Description                    | Initial value |
|--------|------|------------------|--------------------------------|---------------|
| 0x1800 | RW   | WC_ENTRY_0       | WC MAC address with WCID=0     | 0x0           |
| 0x1808 | RW   | WC_ENTRY_1       | WC MAC address with WCID=1     | 0x0           |
| ...    | RW   | ...              | WC MAC address with WCID=2~253 | 0x0           |
| 0x1FF0 | RW   | WC_ENTRY_2<br>54 | WC MAC address with WCID=254   | 0x0           |
| 0x1FF8 | RW   | WC_ENTRY_2<br>55 | Reserved (shall not be used)   | 0x0           |

**Note1:** WCID=Wireless Client ID

### 3.3.1.5 Security table/CIS/Beacon/NULL frame (base : 1018\_0000, offset: 0x4000)

#### 3.3.2 Security Key Format (8DW)

| Offset | Type | Name       | Description            | Initial value |
|--------|------|------------|------------------------|---------------|
| 0x00   | RW   | SECKEY_DW0 | Security key byte3~0   | *             |
| 0x04   | RW   | SECKEY_DW1 | Security key byte7~4   | *             |
| 0x08   | RW   | SECKEY_DW2 | Security key byte11~8  | *             |
| 0x0C   | RW   | SECKEY_DW3 | Security key byte15~12 | *             |
| 0x10   | RW   | TXMIC_DW0  | TX MIC key byte3~0     | *             |
| 0x14   | RW   | TXMIC_DW1  | TX MIC key byte7~4     | *             |
| 0x18   | RW   | RXMIC_DW0  | RX MIC key byte3~0     | *             |
| 0x1C   | RW   | RXMIC_DW1  | RX MIC key byte7~4     | *             |

Note:

1. FOR WEP40, CKIP40, ONLY BYTE4~0 OF SECURITY KEY ARE VALID.
2. For WEP104, CKIP104, only byte12~0 of security key are valid.
3. For TKIP, AES, all the bytes of security key are valid.
4. TX/RX MIC key is used only for TKIP MIC calculation.

#### 3.3.3 IV/EIV format (2 DW)

When TXINFO.WIV=0, hardware will auto lookup IV/EIV from this table and update IV/EIV after encryption is finished.

| Offset | Type | Name       | Description | Initial value |
|--------|------|------------|-------------|---------------|
| 0x00   | RW   | IV_FIELED  | IV field    | *             |
| 0x04   | RW   | EIV_FIELED | EIV field   | *             |

**Note1:** The key index and extension IV bit shall be initialized by software. The MSB octet of IV will not be modified by hardware.

**Note2:** IV/EIV packet number (PN) counter modes:

- a. For WEP40, WEP104, CKIP40, CKIP104, CKIP128 mode, PN=IV[23:0]. EIV[31:0] is not used.
- b. For TKIP mode, PN = {EIV[31:0], IV[7:0], IV[23:16]}, IV[15:8]=(IV[7:0] | 0x20) & 0x7f is generated by hardware.
- c. For AES-CCMP, PN = {EIV[31:0], IV[15:0]}.
- d. PN = PN + 1 after each encryption.

**Note3:** Software may initialize the PN counter to any value.

### 3.3.4 WCID attribute entry format (1DW)

| Offset | Type | Name         | Description                                                                                                                                   | Initial value |
|--------|------|--------------|-----------------------------------------------------------------------------------------------------------------------------------------------|---------------|
| 31:10  | -    | -            | Reserved                                                                                                                                      | *             |
| 9:7    | RW   | RXWI_UDF     | RXWI user define field<br>This field is tagged in the RXWI.UDF fields for the WCID.                                                           | *             |
| 6:4    | RW   | BSS_IDX      | Multiple-BSS index for the WCID                                                                                                               | *             |
| 3:1    | RW   | RX_PKEY_MODE | Pair-wise key security mode<br><br>0: No security<br>1: WEP40<br>2: WEP104<br>3: TKIP<br>4: AES-CCMP<br>5: CKIP40<br>6: CKIP104<br>7: CKIP128 | *             |
| 0      | RW   | RX_PKEY_EN   | Key table selection<br><br>0: shared key table<br>1: pair-wise key table                                                                      | *             |

### 3.3.5 Share key mode entry format (1DW)

| Bits  | Type | Name         | Description                  | Initial Value |
|-------|------|--------------|------------------------------|---------------|
| 31    | -    | -            | Reserved                     | *             |
| 30:28 | RW   | SKEY_MODE_7+ | Shared key7+(8x) mode, x=0~3 | *             |
| 27    | -    | -            | Reserved                     | *             |
| 26:24 | RW   | SKEY_MODE_6+ | Shared key6+(8x) mode, x=0~3 | *             |
| 23    | -    | -            | Reserved                     | *             |
| 22:20 | RW   | SKEY_MODE_5+ | Shared key5+(8x) mode, x=0~3 | *             |
| 19    | -    | -            | Reserved                     | *             |
| 18:16 | RW   | SKEY_MODE_4+ | Shared key4+(8x) mode, x=0~3 | *             |
| 15    | -    | -            | Reserved                     | *             |
| 14:12 | RW   | SKEY_MODE_3+ | Shared key3+(8x) mode, x=0~3 | *             |
| 11    | -    | -            | Reserved                     | *             |
| 10:8  | RW   | SKEY_MODE_2+ | Shared key2+(8x) mode, x=0~3 | *             |
| 7     | -    | -            | Reserved                     | *             |
| 6:4   | RW   | SKEY_MODE_1+ | Shared key1+(8x) mode, x=0~3 | *             |
| 3     | -    | -            | Reserved                     | *             |
| 2:0   | RW   | SKEY_MODE_0  | Shared key0+(8x) mode, x=0~3 | *             |



|  |  |    |  |  |
|--|--|----|--|--|
|  |  | 0+ |  |  |
|--|--|----|--|--|

Key mode definition:

- 0: No security
- 1: WEP40
- 2: WEP104
- 3: TKIP
- 4: AES-CCMP
- 5: CKIP40
- 6: CKIP104
- 7: CKIP128

#### 5.17.7.1 Security Table

#### 3.3.6 Pair-wise key table (offset: 0x4000)

| Offset | Type | Name     | Description                          | Initial value |
|--------|------|----------|--------------------------------------|---------------|
| 0x4000 | RW   | PKEY_0   | Pair-wise key for WCID0              | *             |
| 0x4020 | RW   | PKEY_1   | Pair-wise key for WCID1              | *             |
| ....   | RW   | ....     | Pair-wise key for WCID2~253          | *             |
| 0x5FC0 | RW   | PKEY_254 | Pair-wise key for WCID254            | *             |
| 0x5FE0 | RW   | PKEY_255 | Pair-wise key for WCID255 (not used) | *             |

#### 3.3.7 IV/EIV table (offset: 0x6000)

| Offset | Type | Name      | Description                   | Initial value |
|--------|------|-----------|-------------------------------|---------------|
| 0x6000 | RW   | IVEIV_0   | IV/EIV for WCID0              | *             |
| 0x6008 | RW   | IVEIV_1   | IV/EIV for WCID1              | *             |
| ....   | RW   | ....      | IV/EIV for WCID2~253          | *             |
| 0x67F0 | RW   | IVEIV_254 | IV/EIV for WCID254            | *             |
| 0x67F8 | RW   | IVEIV_255 | IV/EIV for WCID255 (not used) | *             |

#### 3.3.8 WCID attribute table (offset: 0x6800)

| Offset | Type | Name          | Description                  | Initial value |
|--------|------|---------------|------------------------------|---------------|
| 0x6800 | RW   | WCID_ATTR_0   | WCID Attribute for WCID0     | *             |
| 0x6804 | RW   | WCID_ATTR_1   | WCID Attribute for WCID1     | *             |
| ....   | RW   | ....          | WCID Attribute for WCID2~253 | *             |
| 0x6BF8 | RW   | WCID_ATTR_254 | WCID Attribute for WCID254   | *             |
| 0x6BFC | RW   | WCID_ATTR_255 | WCID Attribute for WCID255   | *             |

#### 3.3.9 Shared Key Table (offset: 0x6C00)

| Offset | Type | Name   | Description                         | Initial value |
|--------|------|--------|-------------------------------------|---------------|
| 0x6C00 | RW   | SKEY_0 | Shared key for BSS_IDX=0, KEY_IDX=0 | *             |
| 0x6C20 | RW   | SKEY_1 | Shared key for BSS_IDX=0, KEY_IDX=1 | *             |
| 0x6C40 | RW   | SKEY_2 | Shared key for BSS_IDX=0, KEY_IDX=2 | *             |
| 0x6C60 | RW   | SKEY_3 | Shared key for BSS_IDX=0, KEY_IDX=3 | *             |
| 0x6C80 | RW   | SKEY_4 | Shared key for BSS_IDX=1, KEY_IDX=0 | *             |
| 0x6CA0 | RW   | SKEY_5 | Shared key for BSS_IDX=1, KEY_IDX=1 | *             |
| 0x6CC0 | RW   | SKEY_6 | Shared key for BSS_IDX=1, KEY_IDX=2 | *             |

|        |    |         |                                     |   |
|--------|----|---------|-------------------------------------|---|
| 0x6CE0 | RW | SKEY_7  | Shared key for BSS_IDX=1, KEY_IDX=3 | * |
| 0x6D00 | RW | SKEY_8  | Shared key for BSS_IDX=2, KEY_IDX=0 | * |
| 0x6D20 | RW | SKEY_9  | Shared key for BSS_IDX=2, KEY_IDX=1 | * |
| 0x6D40 | RW | SKEY_10 | Shared key for BSS_IDX=2, KEY_IDX=2 | * |
| 0x6D60 | RW | SKEY_11 | Shared key for BSS_IDX=2, KEY_IDX=3 | * |
| 0x6D80 | RW | SKEY_12 | Shared key for BSS_IDX=3, KEY_IDX=0 | * |
| 0x6DA0 | RW | SKEY_13 | Shared key for BSS_IDX=3, KEY_IDX=1 | * |
| 0x6DC0 | RW | SKEY_14 | Shared key for BSS_IDX=3, KEY_IDX=2 | * |
| 0x6DE0 | RW | SKEY_15 | Shared key for BSS_IDX=3, KEY_IDX=3 | * |
| 0x6E00 | RW | SKEY_16 | Shared key for BSS_IDX=4, KEY_IDX=0 | * |
| 0x6E20 | RW | SKEY_17 | Shared key for BSS_IDX=4, KEY_IDX=1 | * |
| 0x6E40 | RW | SKEY_18 | Shared key for BSS_IDX=4, KEY_IDX=2 | * |
| 0x6E60 | RW | SKEY_19 | Shared key for BSS_IDX=4, KEY_IDX=3 | * |
| 0x6E80 | RW | SKEY_20 | Shared key for BSS_IDX=5, KEY_IDX=0 | * |
| 0x6EA0 | RW | SKEY_21 | Shared key for BSS_IDX=5, KEY_IDX=1 | * |
| 0x6EC0 | RW | SKEY_22 | Shared key for BSS_IDX=5, KEY_IDX=2 | * |
| 0x6EE0 | RW | SKEY_23 | Shared key for BSS_IDX=5, KEY_IDX=3 | * |
| 0x6F00 | RW | SKEY_24 | Shared key for BSS_IDX=6, KEY_IDX=0 | * |
| 0x6F20 | RW | SKEY_25 | Shared key for BSS_IDX=6, KEY_IDX=1 | * |
| 0x6F40 | RW | SKEY_26 | Shared key for BSS_IDX=6, KEY_IDX=2 | * |
| 0x6F60 | RW | SKEY_27 | Shared key for BSS_IDX=6, KEY_IDX=3 | * |
| 0x6F80 | RW | SKEY_28 | Shared key for BSS_IDX=7, KEY_IDX=0 | * |
| 0x6FA0 | RW | SKEY_29 | Shared key for BSS_IDX=7, KEY_IDX=1 | * |
| 0x6FC0 | RW | SKEY_30 | Shared key for BSS_IDX=7, KEY_IDX=2 | * |
| 0x6FE0 | RW | SKEY_31 | Shared key for BSS_IDX=7, KEY_IDX=3 | * |

### 3.3.10 Shared Key Mode (offset: 0x7000)

| Offset | Type | Name            | Description                   | Initial value |
|--------|------|-----------------|-------------------------------|---------------|
| 0x7000 | RW   | SKEY_MODE_0_7   | Shared mode for SKEY0-SKEY7   | *             |
| 0x7004 | RW   | SKEY_MODE_8_15  | Shared mode for SKEY8-SKEY15  | *             |
| 0x7008 | RW   | SKEY_MODE_16_23 | Shared mode for SKEY16-SKEY23 | *             |
| 0x700C | RW   | SKEY_MODE_24_31 | Shared mode for SKEY24-SKEY31 | *             |

### 3.3.10.1 5.17.8 Descriptor and Wireless information

#### 5.17.8.0 TX frame information

To transmit a frame, the driver needs to prepare the TX frame information for hardware. The TX frame information contains the transmission control, the header, and the payload. The transmission control information (the “**TXWI**”) is used by the MAC and BBP and is applied for the associated TX frame when transmission. The header and payload is the content of an 802.11 packet.

The TX information could be scattered in several segments. The TX descriptor (the “**TXD**”) specifies the location and length of the TX frame information segment. TX frame

information could be linked by use of several TXD. These TXD are arranged in a TXD ring in serial. Below diagram illustrates the linking between TXD and TX frame information.

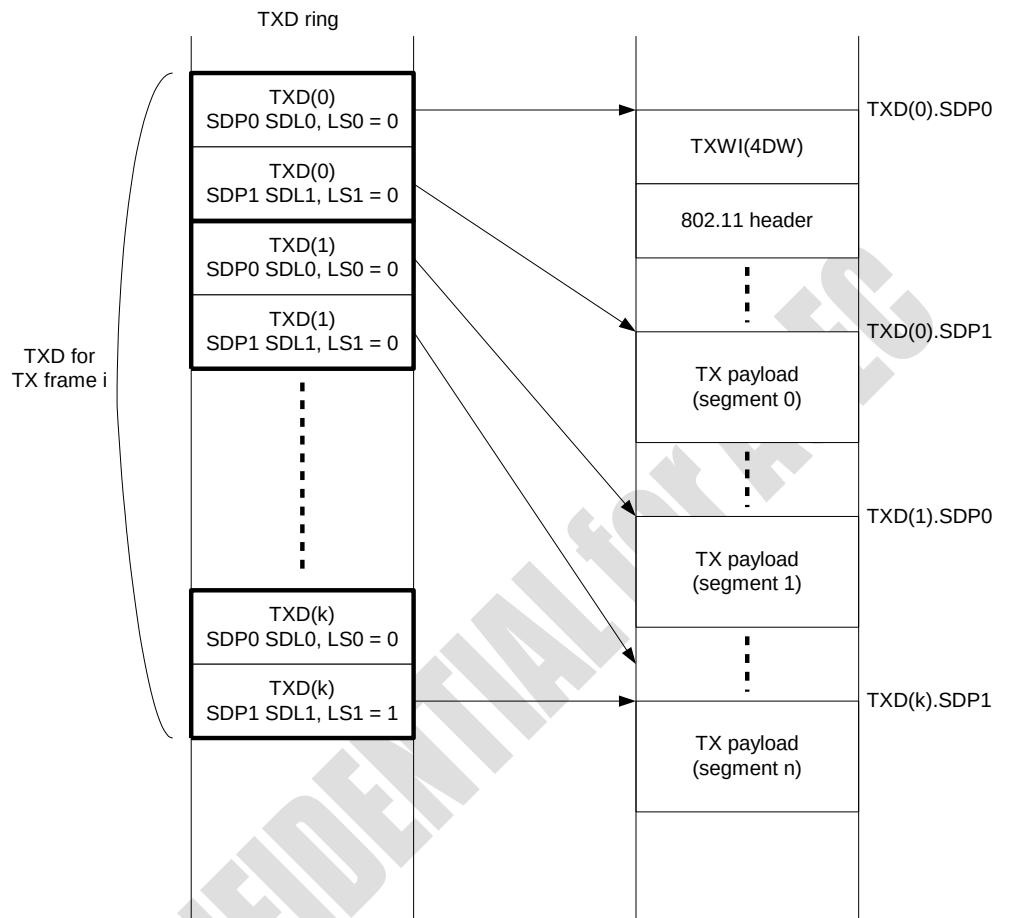


Fig. 5-17-3 TX frame information

#### 5.17.8.1 TX descriptor format

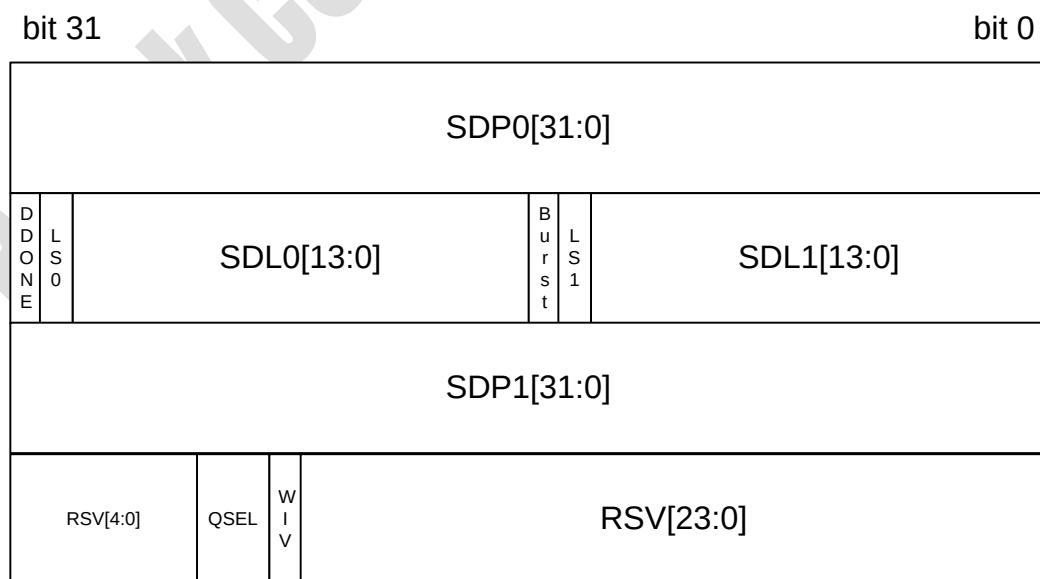
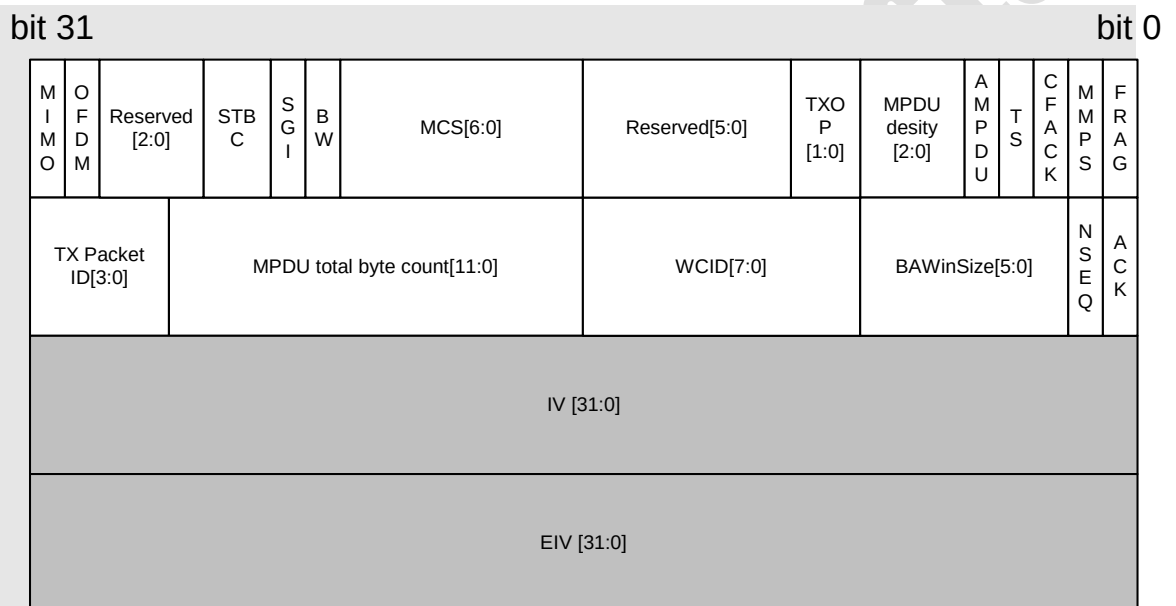


Fig. 5-17-4 TX descriptor format

- ◆ **SDP0** : Segment Data Pointer 0.
- ◆ **SDL0** : Segment Data Length for the data pointed by SDP0.
- ◆ **SDP1** : Segment Data Pointer 1.
- ◆ **SDL1** : Segment Data Length for the data pointed by SDP1.
- ◆ **LS0** : data pointed by SDP0 is the last segment
- ◆ **LS1** : data pointed by SDP1 is the last segment
- ◆ **DDONE** : DMA Done. DMA has transferred the segments pointed by this TX descriptor
- ◆ **Burst**: force DMA to access next TX frame from the same queue.
- ◆ **QSEL**: the ID of the on-chip queue that the TX frame is moved into. 0: MGMT queue, 1: HCCA queue, 2: EDCA queue, 3: unused.
- ◆ **WIV**: 1: driver prepared all 16-byte TXWI. 0: driver prepared only the first 8-byte TXWI.

#### 5.17.8.2 TXWI format



**Fig. 5-17-5 TXWI format**

- ◆ **FRAG**: 1: to inform TKIP engine this is a fragment, so that TKIP MIC is appended by driver at the last fragment; hardware TKIP engine only need to insert IV/EIV and ICV.
- ◆ **MMPS**: 1: the remote peer is in dynamic MIMO-PS mode
- ◆ **CFACK**: 1: if an ACK is required to the same peer as this outgoing DATA frame, then MAC TX will send a single DATA+CFACK frame instead of separate ACK and DATA frames. 0: no piggyback ACK allowed for the RA of this frame.
- ◆ **TS**: 1: This is a BEACON or ProbeResponse frame and MAC needs to auto insert 8-byte timestamp after 802.11 WLAN header.
- ◆ **AMPDU**: this frame is eligible for AMPDU. MAC TX will aggregate subsequent outgoing frames having <same RA, same TID, AMPDU=1> whenever TXOP allows. Even there's only one DATA frame to be sent, as long as the AMPDU bit in TXWI is ON, MAC will still package it as AMPDU with implicit BAR. This adds only 4-byte AMPDU delimiter overhead into the outgoing frame and imply the response frame is a BA instead of ACK. NOTE: driver should set AMPDU=1 only after a BA session is successfully negotiated, because Block ACK is the only way to acknowledge in AMPDU case.
- ◆ **MPDU density**: 1/4usec ~ 16usec per-peer parameter used in outgoing A-MPDU. (This field complies with the "minimum MDPU Starting Spacing" of the A-MPDU parameter field of draft 1.08).  
000- no restriction  
001- 1/4  $\mu$ sec  
010- 1/2  $\mu$ sec

011- 1  $\mu$ sec  
100- 2  $\mu$ sec  
101- 4  $\mu$ sec  
110- 8  $\mu$ sec  
111- 16  $\mu$ sec

- ◆ **TXOP**: TX back off mode. 0: HT TXOP rule; 1: PIFS TX; 2: SIFS (only when previous frame exchange is successful); 3: Back off.
- ◆ **"MCS/BW/ShortGI/OFDM/MIMO"**: TX data rate & MIMO parameters for this outgoing frame to be filled into BBP
- ◆ **ACK**: this bit informs MAC to wait for ACK or not after transmission of the frame. Event though QOD DATA frame has ACK policy in its QOS CONTROL field, MAC TX solely depends on this ACK bit to decide waiting of ACK or not.
- ◆ **NSEQ**: 1: to use the special h/w SEQ number register in MAC block.
- ◆ **BA window size**: tell MAC the maximum number of to-be-BAed frames is allowed of the RA (RA's BA re-ordering buffer size)
- ◆ **WCID (Wireless Client Index)** : lookup result of ADDR1 in the peer table (255=not found). This index is also used to find all the attributes of the wireless peer (e.g. TX rate, TX power, pair-wise KEY, IV, EIV,). This index has consistent meaning in both driver and hardware.
- ◆ **MSDU total byte count**: total length of this frame.
- ◆ **Packet ID**: as a cookie specified by driver and will be latched into the TX result register stack. Driver use this field to identify special frame's TX result.
- ◆ **IV**: used by encryption engine.
- ◆ **EIV**: used by encryption engine.

### 5.17.8.3 RX descriptor ring

The RX descriptor (the "**RXD**") specifies the location to place the payload of the received frame (the RX payload) and the associated receiving information (the "**RXWI**"). One RXD serves for one receiving frame. Only SDP0 and SDL0 are useful in the RXD. The RXD is arranged in the RXD ring in serial. The hardware links the RXWI and RX payload in serial and place it to the location specified in SDP0. See below diagram.

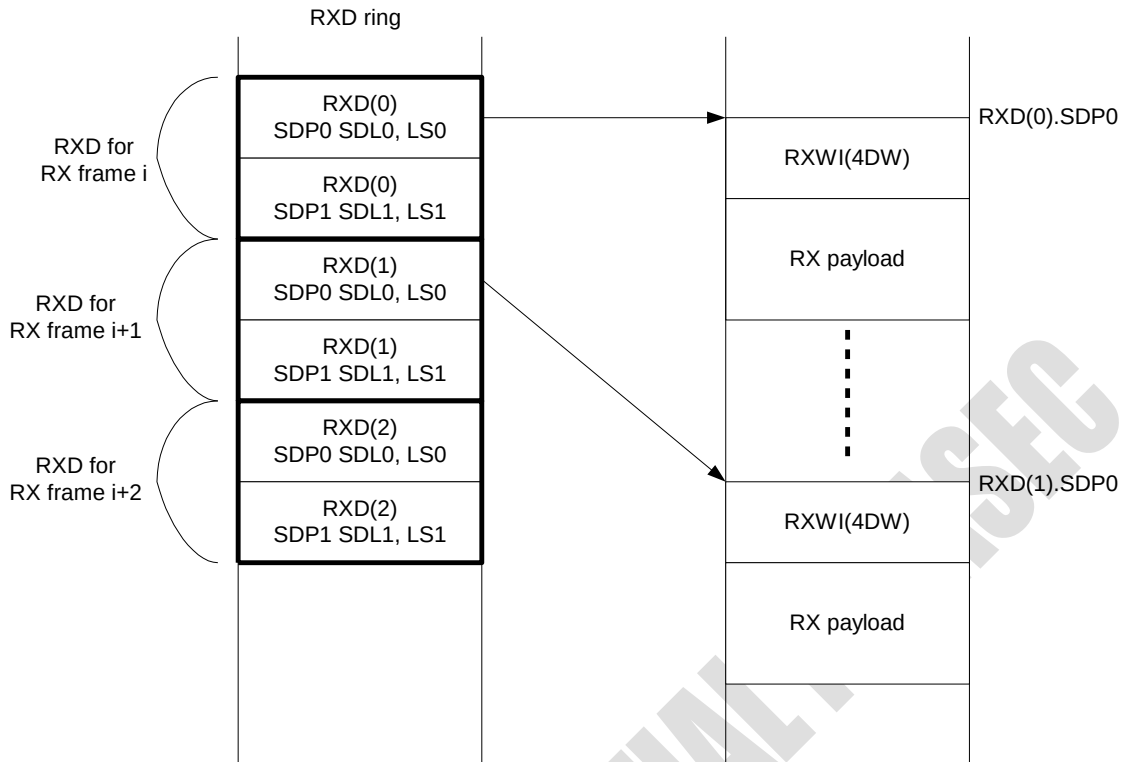


Fig. 5-17-6 RX descriptor ring

#### 5.17.8.4 RX descriptor format

bit 31

bit 0

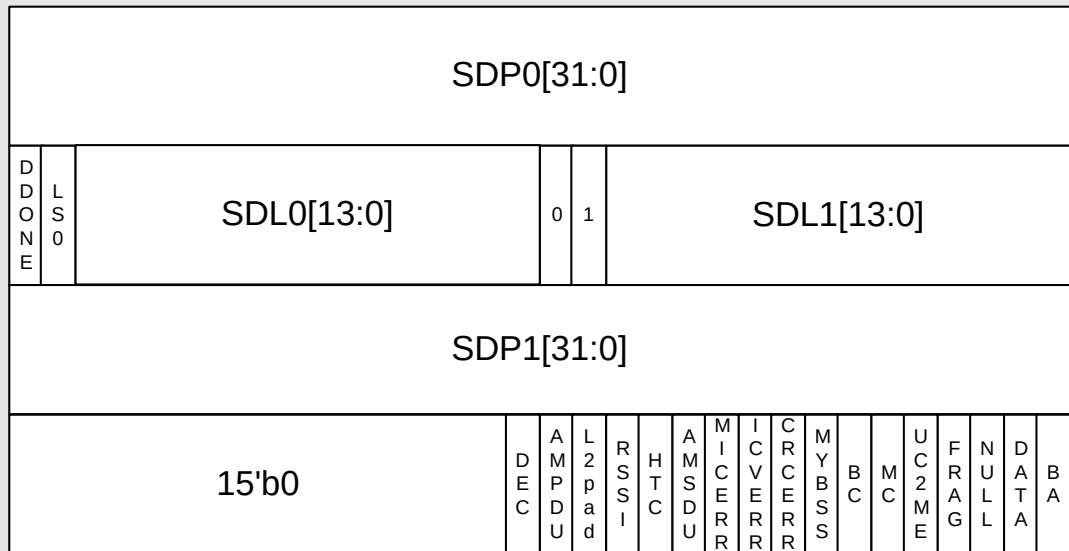


Fig. 5-17-7 RX descriptor format

Following fields are driver-specified.

- ◆ **SDP0** : Segment Data Pointer 0.
- ◆ **SDL0** : Segment Data Length for the data pointed by SDP0.
- ◆ **SDP1** : Segment Data Pointer 1.
- ◆ **SDL1** : Segment Data Length for the data pointed by SDP1.
- ◆ **DDONE** : DMA Done. DMA has moved the RX frame to the specified location. Set by hardware and cleared by driver.

Following fields are filled by hardware.

- ◆ **BA**: the received frame is part of BA session, need to do re-ordering
- ◆ **DATA**: 1: the received frame is DATA type
- ◆ **NULL**: 1: the received frame has sub-type NULL/QOS-NULL
- ◆ **FRAG**: 1: the receive frame is a fragment
- ◆ **UC2ME**: 1: the received frame ADDR1 = my MAC address
- ◆ **MC**: 1: the received frame ADDR1 = multicast
- ◆ **BC**: 1: the received frame ADDR1 = ff:ff:ff:ff:ff:ff
- ◆ **MyBSS**: 1: the received frame BSSID is one of my BSS (as an AP, max 4 BSSID supported)
- ◆ **CRC error**: 1: the received frame is CRC error
- ◆ **ICV error**: 1: the received frame is ICV error
- ◆ **MIC error**: 1: the received frame is MIC error (RX CNRL register should support individual pass-up error frame to driver in order to implement MIC error detection feature)
- ◆ **AMSDU**: the received frame is in A-MSDU sub frame format which is <802.3 + MSDU + padding>
- ◆ **HTC**: 1: this received frame came with HTC field, 0: no HTC field
- ◆ **RSSI**: 1: RSSI information available in RSSI0, RSSI1, RSSI2 fields
- ◆ **L2Pad**: 1: the L2 header is recognizable and been 2-byte-padded to ensure payload to align at 4-byte boundary. 0: L2 header not extra padded
- ◆ **AMPDU**: 1: this is an AMPDU segregated frame
- ◆ **DEC**: 1: this is a decrypted frame

#### 5.17.8.5 RXWI format

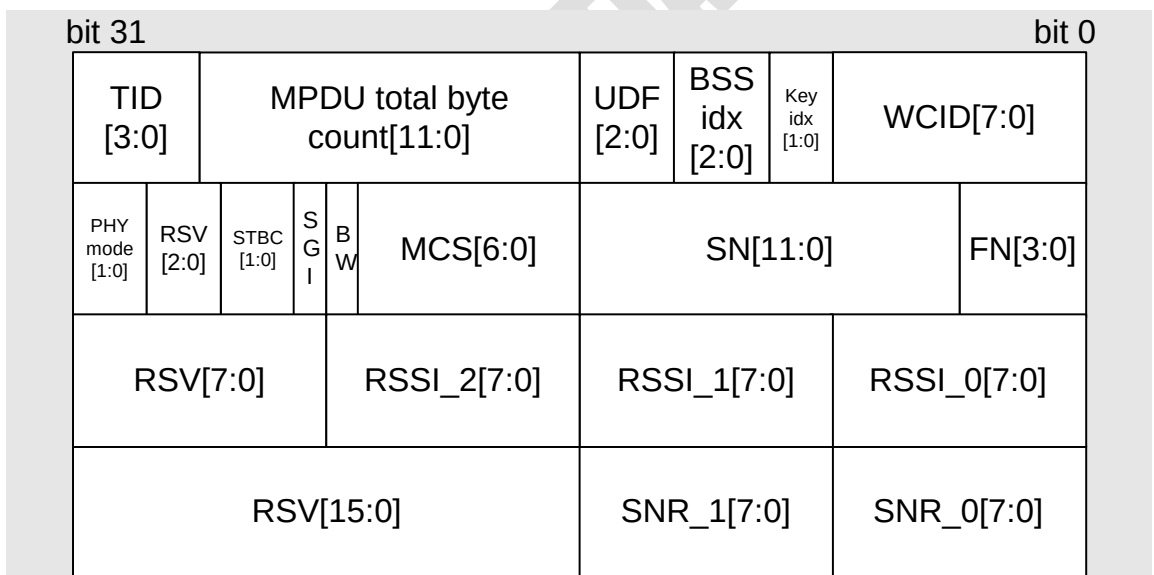


Fig. 5-17-8 RXWI format

- ◆ **WCID**: index of ADDR2 in the pair wise KEY table. This value uniquely identifies the TA. WCID=255 means not found.
- ◆ **KEY Index**: 0~3 extracted from IV field. For driver reference only, no particular usage so far.
- ◆ **BSSID index**: 0~7 for BSSID0~7. Extract from 802.11 header (the last three bits of BSSID field).
- ◆ **UDF**: User Defined Field.
- ◆ **MPDU total byte count**: the entire MPDU length.
- ◆ **TID**: extracted from 802.11 QOS control field.
- ◆ **FN**: fragment number of the received MPDU. Extract from 802.11 header.
- ◆ **SN**: sequence number of the received MPDU. Used for BA re-ordering especially that AMSDU are auto segregated by hardware and lost the 802.11 header.
- ◆ **"MCS/BW/SI/PHYmode"**: RX data rate & related MIMO parameters of this frame got from PLCP header. See next section for the detail.

- ◆ **RSSI0, RSSI1, RSSI2**: BBP reported RSSI information of the received frame.
- ◆ **SNR0, SNR1**: BBP reported SNR information of the received frame.

#### 5.17.8.6 Brief PHY rate format and definition

A 16-bit brief PHY rate is used in MAC hardware.  
It is the same PHY rate field described in TXWI and RXWI.

| Bit   | Name     | Description                                                                                                            |
|-------|----------|------------------------------------------------------------------------------------------------------------------------|
| 15:14 | PHY MODE | Preamble mode<br>0: Legacy CCK, 1: Legacy OFDM,<br>2: HT mix mode, 3: HT green field                                   |
| 13:11 | -        | Reserved                                                                                                               |
| 10:9  | -        | Reserved                                                                                                               |
| 8     | SGI      | Short Guard Interval, only support for HT mode<br>0: 800ns, 1: 400ns                                                   |
| 7     | BW       | Bandwidth<br>Support both legacy and HT modes<br>40Mhz in legacy mode means duplicate legacy<br><br>0: 20Mhz, 1: 40Mhz |
| 6:0   | MCS      | Modulation Coding Scheme                                                                                               |

Table. Brief PHY rate format

| MODE = Legacy CCK                                                                               |                                            |
|-------------------------------------------------------------------------------------------------|--------------------------------------------|
| MCS = 0                                                                                         | Long Preamble CCK 1Mbps                    |
| MCS = 1                                                                                         | Long Preamble CCK 2Mbps                    |
| MCS = 2                                                                                         | Long Preamble CCK 5.5Mbps                  |
| MCS = 3                                                                                         | Long Preamble CCK 11Mbps                   |
| MCS = 8                                                                                         | Short Preamble CCK 1Mbps<br>* illegal rate |
| MCS = 9                                                                                         | Short Preamble CCK 2Mbps                   |
| MCS = 10                                                                                        | Short Preamble 5.5Mbps                     |
| MCS = 11                                                                                        | Short Preamble 11Mbps                      |
| Other MCS codes are reserved in legacy CCK mode.<br>BW and SGI are reserved in legacy CCK mode. |                                            |
| MODE = Legacy OFDM                                                                              |                                            |
| MCS = 0                                                                                         | 6Mbps                                      |
| MCS = 1                                                                                         | 9Mbps                                      |
| MCS = 2                                                                                         | 12Mbps                                     |
| MCS = 3                                                                                         | 18Mbps                                     |
| MCS = 4                                                                                         | 24Mbps                                     |
| MCS = 5                                                                                         | 36Mbps                                     |
| MCS = 6                                                                                         | 48Mbps                                     |
| MCS = 7                                                                                         | 54Mbps                                     |



|                                                                                |                                  |
|--------------------------------------------------------------------------------|----------------------------------|
| Other MCS code in legacy CCK mode are reserved                                 |                                  |
| When BW = 1, duplicate legacy OFDM is sent.                                    |                                  |
| SGI is reserved in legacy OFDM mode.                                           |                                  |
| MODE = HT mix mode / HT green field                                            |                                  |
| MCS = 0 (1S)                                                                   | (BW=0, SGI=0) 6.5Mbps            |
| MCS = 1                                                                        | (BW=0, SGI=0) 13Mbps             |
| MCS = 2                                                                        | (BW=0, SGI=0) 19.5Mbps           |
| MCS = 3                                                                        | (BW=0, SGI=0) 26Mbps             |
| MCS = 4                                                                        | (BW=0, SGI=0) 39Mbps             |
| MCS = 5                                                                        | (BW=0, SGI=0) 52Mbps             |
| MCS = 6                                                                        | (BW=0, SGI=0) 58.5Mbps           |
| MCS = 7                                                                        | (BW=0, SGI=0) 65Mbps             |
| MCS = 8 (2S)                                                                   | (BW=0, SGI=0) 13Mbps             |
| MCS = 9                                                                        | (BW=0, SGI=0) 26Mbps             |
| MCS = 10                                                                       | (BW=0, SGI=0) 39Mbps             |
| MCS = 11                                                                       | (BW=0, SGI=0) 52Mbps             |
| MCS = 12                                                                       | (BW=0, SGI=0) 78Mbps             |
| MCS = 13                                                                       | (BW=0, SGI=0) 104Mbps            |
| MCS = 14                                                                       | (BW=0, SGI=0) 117Mbps            |
| MCS = 15                                                                       | (BW=0, SGI=0) 130Mbps            |
| MCS = 32                                                                       | (BW=1, SGI=0) HT duplicate 6Mbps |
| When BW=1, PHY_RATE = PHY_RATE * 2                                             |                                  |
| When SGI=1, PHY_RATE = PHY_RATE * 10/9                                         |                                  |
| The effects of BW and SGI are accumulative.                                    |                                  |
| When MCS=0~7(1S), SGI option is supported. BW option is supported.             |                                  |
| When MCS=8~15(2S), SGI option is supported. BW option is supported.            |                                  |
| When MCS=32, only SGI option is supported. BW option is not supported. (BW =1) |                                  |
| Other MCS code in HT mode are reserved                                         |                                  |

### 3.3.10.2 5.17.9 Driver implementation note

#### 5.17.9.0 Instruction of down load 8051 firmware

1. Select on-chip program memory
  - i. SYS\_CTRL.HST\_PM\_SEL (0x0400.bit[16]) = 1
2. Write firmware into program memory space, which starts at 0x2000.
3. Close on-chip program memory:
  - i. SYS\_CTRL.HST\_PM\_SEL (0x0400.bit[16]) = 0

4. 8051 starts.

#### 5.17.9.1 Instruction of initialize DMA

1. Set base addresses and total number of descriptors:
  - i. TX\_BASE\_PTR0~TX\_BASE\_PTR5
  - ii. RX\_BASE\_PTR
  - iii. TX\_MAX\_CNT0~TX\_MAX\_CNT5
  - iv. RX\_MAX\_CNT
2. Set WMM parameters:
  - i. WMM\_AIFSN\_CFG
  - ii. WMM\_CWMIN\_CFG
  - iii. WMM\_CWMAX\_CFG
  - iv. WMM\_TXOP0\_CFG and WMM\_TXOP1\_CFG
3. Set DMA global configuration except TX\_DMA\_EN and RX\_DMA\_EN bits:
  - i. WPDMA\_GLO\_CFG
4. Set interrupt configuration:
  - i. DELAY\_INT\_CFG
5. Enable DMA interrupt:
  - i. INT\_MASK
6. Enable DMA:
  - i. WPDMA\_GLO\_CFG.TX\_DMA\_EN = 1, WPDMA\_GLO\_CFG.RX\_DMA\_EN = 1

#### 5.17.9.2 Instruction of clock control

##### 3.3.11 5.17.9.2.0 Clock turn-off sequence

1. Switch 80MHz main clock to PLL clock:
  - i. Set SYS\_CTRL.CLKSELECT = 1.
2. Turn clock off:
  - i. Set SYS\_CTRL.MAC\_CLK\_EN = 0.
  - ii. Set SYS\_CTRL.DMA\_CLK\_EN = 0.
3. Turn off PLL:
  - i. Set PWR\_PIN\_CFG.IO\_PLL\_PD = 1.

##### 3.3.12 5.17.9.2.1 Clock turn-on sequence

1. Turn on PLL:
  - i. Set PWR\_PIN\_CFG.IO\_PLL\_PD = 0.
2. Waiting at least \$bbp\_pll\_ready for PLL clock stable.
3. Turn on clock:
  - i. Set SYS\_CTRL.MAC\_CLK\_EN = 1.
  - ii. Set SYS\_CTRL.DMA\_CLK\_EN = 1.

#### 5.17.9.3 Instruction of TX/RX control

##### 3.3.13 5.17.9.3.0 Freeze TX and RX sequence

1. Disable DMA TX:
  - i. Set WPDMA\_GLO\_CFG..TX\_DMA\_EN = 0.
2. Polling until DMA TX becomes idle and PBF TX queue becomes empty:
  - i. Polling WPDMA\_GLO\_CFG. TX\_DMA\_BUSY = 0.
  - ii. Polling TXRXQ\_STA.TX0Q\_STA = 2, TXRXQ\_STA.TX1Q\_STA = 2, polling TXRXQ\_STA.TX2Q\_STA = 2.
  - iii. If the polling period > \$dma\_tx\_polling\_timeout, abort power saving procedure.
3. Disable MAC TX and RX:
  - i. Set MAC\_SYS\_CTRL.MAC\_RX\_EN = 0, MAC\_SYS\_CTRL.MAC\_TX\_EN = 0.

4. Polling until MAC TX and RX is disabled:
  - i. Polling MAC\_STATUS\_REG. TX\_STATUS = 0, MAC\_STATUS\_REG. RX\_STATUS = 0
  - ii. If the polling period > \$mac\_polling\_timeout, abort power saving procedure.
5. Disable DMA RX:
  - i. Set WPDMA\_GLO\_CFG..RX\_DMA\_EN = 0.
6. Polling until both DMA RX becomes idle and PBF RX queue becomes empty:
  - i. Polling WPDMA\_GLO\_CFG. RX\_DMA\_BUSY = 0.
  - ii. Polling TXRXQ\_STA.RX0Q\_STA = 0x22.
  - iii. If the polling period > \$dma\_rx\_polling\_timeout, abort power saving procedure.

#### 3.3.14 5.17.9.3.1 Recover TX and RX sequence

1. Enable DMA TX and RX:
  - i. Set WPDMA\_GLO\_CFG..RX\_DMA\_EN = 1.
  - ii. Set WPDMA\_GLO\_CFG..TX\_DMA\_EN = 1.
2. Enable MAC TX and RX:
  - i. Set MAC\_SYS\_CTRL.MAC\_RX\_EN = 1.
  - ii. Set MAC\_SYS\_CTRL.MAC\_TX\_EN = 1.

#### 15.17.9.4 Instruction of RF power on/off sequence

1. Power down RF components sequence
  - i. Power down RF component
    1. Set PWR\_PIN\_CFG.IO\_ADDA\_PD = 1.
    2. Set PWR\_PIN\_CFG.IO\_RF\_PE = 0.
    3. Set TX\_PIN\_CFG.TRSW\_EN = 0.
    4. Set TX\_PIN\_CFG.RFTR\_EN = 0.
    5. Set TX\_PIN\_CFG.LNA\_PE\*EN = 0.
    6. Set TX\_PIN\_CFG.PA\_PE\*EN = 0.
2. Enable RF components sequence
  - i. Recover the registers in previous sequence.
  - ii. Wait \$rf\_pll\_ready for RF PLL becomes stable.

#### 15.17.9.5 Power saving procedure

1. Freeze TX and RX
2. Power down LED and RF components
3. Clock turn-off

#### 15.17.9.6 Power recovery procedure

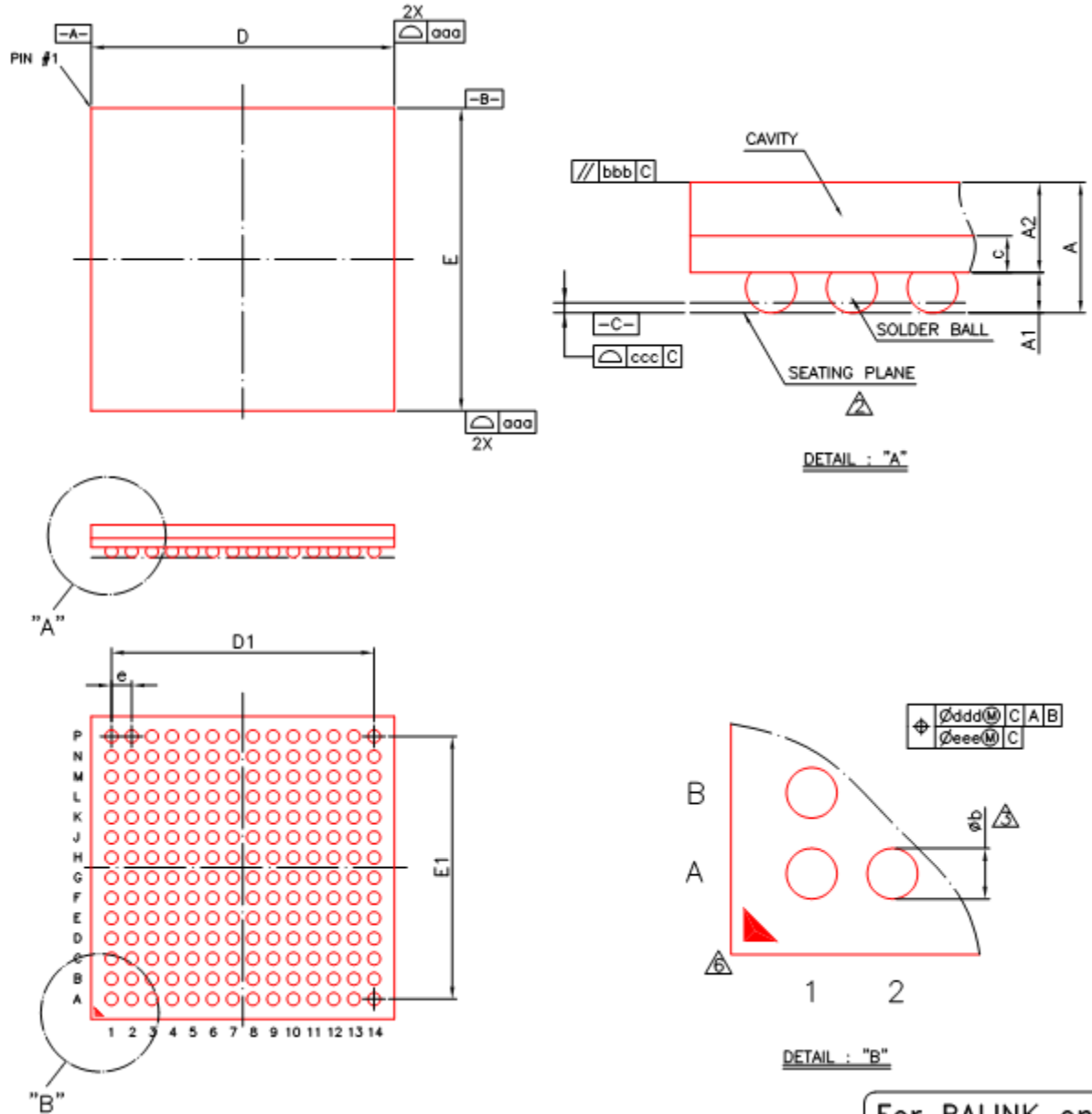
1. Clock turn-on
2. Enable LED and RF components
3. Recover TX and RX

#### 15.17.9.7 Parameters

1. \$rf\_pll\_ready = TBD.
2. \$bbp\_pll\_ready = 500 us.
3. \$dma\_rx\_polling\_timeout = TBD.
4. \$dma\_tx\_polling\_timeout = TBD.
5. \$mac\_polling\_timeout = TBD.

#### 4 Package Physical Dimension

##### 4.1 TFBGA 196B (12×12×0.94mm)



For RALINK only

| Symbol | Dimension in mm |       |       | Dimension in inch |       |       |
|--------|-----------------|-------|-------|-------------------|-------|-------|
|        | MIN             | NOM   | MAX   | MIN               | NOM   | MAX   |
| A      | ---             | ---   | 1.40  | ---               | ---   | 0.055 |
| A1     | 0.35            | 0.40  | 0.45  | 0.014             | 0.016 | 0.018 |
| A2     | 0.84            | 0.89  | 0.94  | 0.033             | 0.035 | 0.037 |
| c      | 0.32            | 0.36  | 0.40  | 0.013             | 0.014 | 0.016 |
| D      | 11.90           | 12.00 | 12.10 | 0.469             | 0.472 | 0.476 |
| E      | 11.90           | 12.00 | 12.10 | 0.469             | 0.472 | 0.476 |
| D1     | ---             | 10.40 | ---   | ---               | 0.409 | ---   |
| E1     | ---             | 10.40 | ---   | ---               | 0.409 | ---   |
| e      | ---             | 0.80  | ---   | ---               | 0.031 | ---   |
| b      | 0.45            | 0.50  | 0.55  | 0.018             | 0.020 | 0.022 |
| aaa    | 0.15            |       |       | 0.006             |       |       |
| bbb    | 0.20            |       |       | 0.008             |       |       |
| ccc    | 0.20            |       |       | 0.008             |       |       |
| ddd    | 0.15            |       |       | 0.006             |       |       |
| eee    | 0.08            |       |       | 0.003             |       |       |
| MD/ME  | 14/14           |       |       | 14/14             |       |       |

**NOTE :**

1. CONTROLLING DIMENSION : MILLIMETER.

△ PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

△ DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.

4. THERE SHALL BE A MINIMUM CLEARANCE OF 0.25mm BETWEEN THE EDGE OF THE SOLDER BALL AND THE BODY EDGE.

5. SPECIAL CHARACTERISTICS C CLASS: bbb, ccc

△ THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY.

**5 Revision History**

| Rev | Date       | From     | Description     |
|-----|------------|----------|-----------------|
| 0.0 | 2010/01/12 | James hu | Initial Release |
|     |            |          |                 |
|     |            |          |                 |

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